Technical Manual

ELECTRO INST.

MODEL 630
DIGITAL MULTIMETER
INSTRUCTION MANUAL

Honeywell

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MODEL 630
DIGITAL MULTIMETER
INSTRUCTION MANUAL

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MODEL 630 DIGITAL MULTIMETER

CHANGE NOTICE NO. 1

The following change applies to the Model 630 Digital Multimeter Instruction Manual.

Paragraph 2.7, Operating procedures for Period or time Interval measurements.

Step c should read: Connect signal cable to HI, LO, and GUARD input jacks at rear rail as illustrated in figure 2.3. If a DC component is present on the input signal, use a blocking capacitor in series with the line to the HI connector, or offset the input signal so the selected slopes of the input waveform will pass through the zero axis.

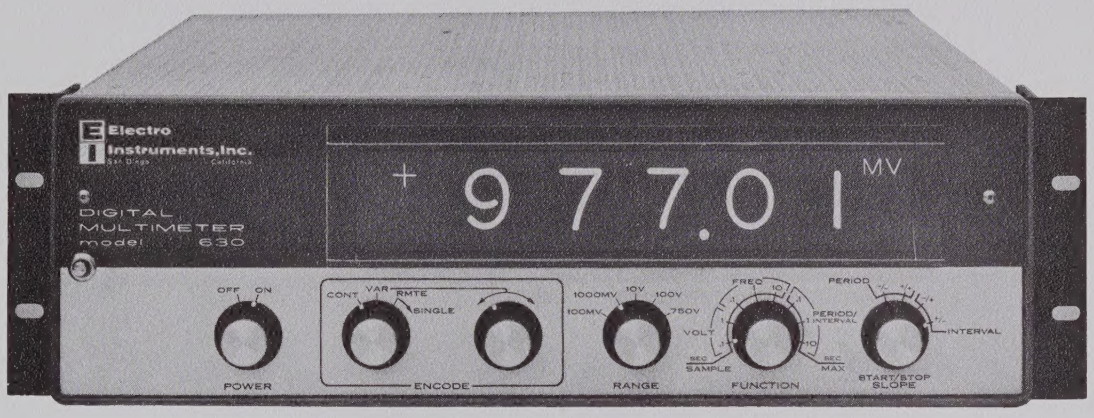
MODEL 630 DIGITAL MULTIMETER

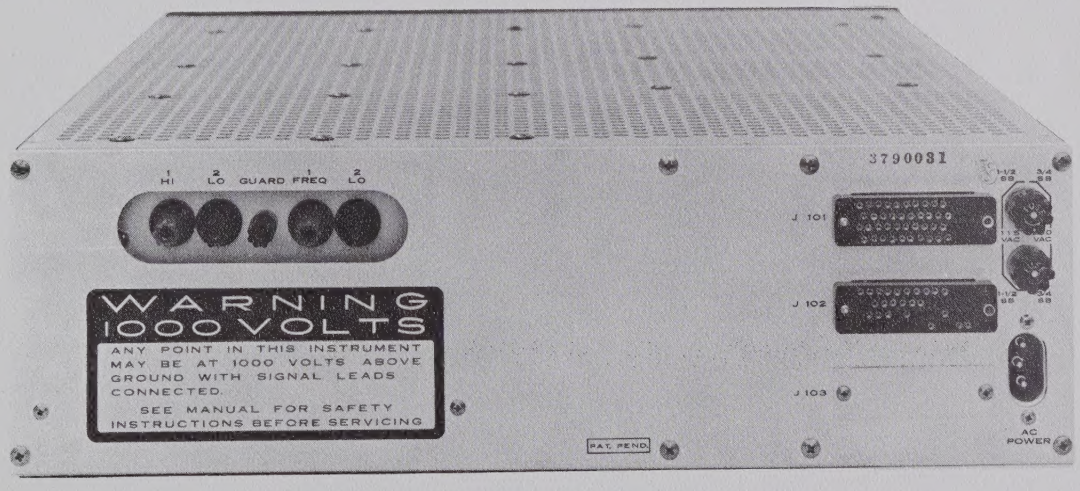
CHANGE NOTICE NO. 2

The following change applies to the Model 630 Digital Multimeter Instruction Manual.

Page 2.8, paragraph 2.7. OPERATING PROCEDURES FOR PERIOD OR TIME INTERVAL MEASUREMENTS

Add between steps a and b the following: "Set RANGE switch to 1000MV"


Electro Instruments, Inc.
San Diego California
DIGITAL MULTIMETER
model 630
+ 977.01 MV
OFF ON
POWER
CONT VAR RMTE SINGLE
ENCODE
1000MV 10V 100V
100MV 750V
VOLT
RANGE
FREQ PERIOD
PERIOD/ INTERVAL
SEC SAMPLE
SEC MAX
FUNCTION
INTERVAL
START/STOP SLOPE


3790031
1 HI
2 LO
GUARD
1 FREQ
2 LO
WARNING
1000 VOLTS
ANY POINT IN THIS INSTRUMENT MAY BE AT 1000 VOLTS ABOVE GROUND WITH SIGNAL LEADS CONNECTED.
SEE MANUAL FOR SAFETY INSTRUCTIONS BEFORE SERVICING
PAT. PEND.
J 101
J 102
J 103
AC POWER

MODEL 630 DIGITAL MULTIMETER

CHANGE NOTICE NO. 2

The following changes apply to the Model 630 Digital Multimeter Instruction Manual for instruments having serial numbers 515 or higher:

a. In Figure 4.1 delete item 43, the reference supply zener current adjustment. The adjustment has been moved to a subassembly on the inside power supply board (item H, Figure 4.1).

b. Step d in paragraph 4.1 should read: Remove the top cover from the instrument. Locate the screwdriver adjustment on the subassembly mounted on the inside power supply board (item H, Figure 4.1). Vary the adjustment until the milliammeter reads the current value specified by the factory for the replacement zener.

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SECTION I

DESCRIPTION

1.1 INTRODUCTION

The Model 630 is a solid-state 5-digit meter capable of measuring DC voltage, frequency, period, and time interval with a single start/stop channel. This precision instrument will measure DC voltages from 0.000001 to 750.00 volts, frequencies from 10 cps to 1 mc, and periods or time intervals from 00.001 milliseconds to 10 seconds. The measurements, with operating mode symbol and correctly placed decimal point are visually displayed by a wide-angle 3-position tilting readout. Corresponding in-line electrical signals in decimal code are presented at output connectors.

Special features include true differential input for all modes, high common and normal mode interference rejection on DC voltage measurements, accurate low-level frequency and period measurements, fast measuring speed, and solid-state reliability.

1.2 APPLICATIONS

The Model 630 offers many possibilities for industrial application. It can be used to measure such physical parameters as vibration, stress, speed, acceleration, rpm, flow, and many other phenomena when converted by suitable transducers to DC voltage, pulse or periodic waveform. Its electrical output, combined with remote control and storage capability make it ideally suited for incorporation in systems.

1.3 EQUIPMENT DESCRIPTION

The Model 630 is housed in a metal case 5-1/4" high, 20-3/4 inches from front to back, and 17 inches wide. Mounting brackets are furnished as standard equipment to permit 19-inch panel rack installation. Internal construction consists largely of modular circuit elements in the form of transistorized plug-in etched boards. All operating controls are conveniently located on the front panel.

1.3.1 Controls and Indicators

POWER switch:

A front panel switch with ON and OFF positions controls AC power to the instrument.

ENCODE controls:

Two front panel controls consisting of a 4-position switch and a variable potentiometer control the encoding rate. For CONT position of the switch the instrument operates at the maximum encode rate; VAR position allows the time between encodings to be adjusted over a range from 0.2 to 5 seconds with the variable control; REMOTE allows the encoding period to be remotely started by application of contact closure between pins z and DD of connector J102; SINGLE position is spring loaded and is used for manually starting the encoding period.

RANGE switch:

A front panel input signal attenuator selector for DC voltage, period, and time interval measurements. The selectable ranges are listed in table 1.1.

Table 1.1 Range Switch Functions

INPUT VOLTAGE RANGE	RANGE SWITCH SET.	FUNCTION SWITCH SET
000.01 to 120.00 MV	100 MV	VOLT 0.1 SEC SAMPLE
00.001 to 120.000 MV	100 MV	VOLT 1 SEC SAMPLE
0000.1 to 1200.0 MV	1000 MV	VOLT 0.1 SEC SAMPLE
000.01 to 1200.00 MV	1000 MV	VOLT 1 SEC SAMPLE
00.001 to 12.000 V	10 V	VOLT 0.1 SEC SAMPLE
0.0001 to 12.0000 V	10 V	VOLT 1 SEC SAMPLE
000.01 to 120.00 V	100 V	VOLT 0.1 SEC SAMPLE
00.001 to 120.000 V	100 V	VOLT 1 SEC SAMPLE
000.1 to 750.0 V	750 V	VOLT 0.1 SEC SAMPLE
000.01 to 750.00 V	750 V	VOLT 1 SEC SAMPLE
300 MV RMS to 50 V P-P	1000 MV	PERIOD/INTERVAL 0.1 SEC MAX
300 MV RMS to 50 V P-P	1000 MV	PERIOD/INTERVAL 1 SEC MAX
300 MV RMS to 50 V P-P	1000 MV	PERIOD/INTERVAL 10 SEC MAX

FUNCTION switch:

A front panel 8-position switch selects operating mode and measurement resolution:

VOLT 0.1 SEC SAMPLE position selects DC voltage mode and an input signal integration time of 1/10 second.

VOLT 1 SEC SAMPLE position selects DC voltage mode and an input signal integration time of 1 second.

FREQ 0.1 SEC SAMPLE position conditions meter for frequency measurements in the range 000.01 kc to 999.99 kc.

FREQ 1 SEC SAMPLE position conditions meter for frequency measurements in the range 00.001 kc to 99.999 kcs.

FREQ 10 SEC SAMPLE position conditions meter for frequency measurements in the range 00.001 kc to 9.9999 kcs.

PERIOD/INTERVAL 0.1 SEC MAX position conditions meter for period or time interval measurements in the range 00.001 millisecond to 99.999 milliseconds.

PERIOD/INTERVAL 1 SEC MAX position conditions meter for period or time interval measurements in the range 000.01 msec to 999.99 msec (1 sec).

PERIOD/INTERVAL 10 SEC MAX position conditions meter for period or time interval measurements in the range 0000.1 msec to 9999.9 msec (10 sec).

START/STOP SLOPE switch:

A front panel switch used in period and time interval measurements to select the point on the input waveform on which the measurement is to start and the point on which it is to stop:

In -/- position the measurement starts as the applied waveform passes through the zero axis in a negative direction and stops as the waveform next passes through the zero axis in a negative direction.

In +/+ position the measurement starts as the applied waveform passes through the zero axis in a positive direction and stops as the waveform next passes through the zero axis in a positive direction.

in +/- position the measurement starts as the applied waveform passes through the zero axis in the positive direction and stops as the waveform next passes through the zero axis in a negative direction.

In -/+ position the measurement starts as the applied waveform passes through the zero axis in a negative direction and stops as the waveform next passes through the zero axis in a positive direction.

+/+ and -/- result in a reading of the period of the waveform. For best accuracy the zero crossings with the steepest rise time should be selected.

READOUT:

A visual display on the front panel consisting of five digits for measurement magnitude indication, decimal point, E symbol for overrange indication on DC voltage measurements, and the following symbols to indicate operating mode:

MV indicates millivolt measurement

V indicates voltage measurement

KC indicates frequency measurement in kilocycles

MS indicates period or time interval measurement in milliseconds

The E symbol is displayed for DC voltage measurements in excess of full scale on any given range. For up to 20% over full scale the readings are valid with the E symbol serving as the most significant digit when a 1-second sample period is used. For example, when E20.000 is displayed the true reading is 120.000 volts. For a 0.1 second sample period the same measurement would be displayed as E120.00 volts. If two diodes are removed from the sample logic board (see paragraph 3.5.2) the correct polarity symbol will display along with the E symbol for valid overrange measurements.

1.3.2 Electrical Connectors

The Model 630 is equipped with two AMP202215-2 female 50-pin connectors (J101 and J102), and five female banana jacks (HI, LO, LO, FREQ, and GUARD). All are located on the rear rail. J101 and J102 supply output information primarily for digital printer or recroder operation. The information consists of five digits of measurement magnitude (in 10-line decimal code for each digit), operating mode indicator (logic voltage levels on selected lines), overrange indicator (logic voltage level), and a print command (positive pulse). Pin z on J102 is an input terminal for remote encode commands (negative going pulse edge or contact closure to ground). Terminal information for these connectors is listed in tables 1.2 and 1.3.

The HI, LO, FREQ, and GUARD input terminals accept the signals being measured. For frequency measurements the high side of the signal line should be connected to the FREQ jack with signal common going to both the LO and GUARD jacks. For period or time interval measurements the high side of the signal line should be connected to the HI jack with common going to both the LO and GUARD jacks. For DC voltage measurements a true differential, guarded, and floating DC

measurement will be provided if the high side of the signal cable is connected to the HI jack, common to the LO jack, and the cable shield to the GUARD jack and to the source of the common mode voltage.

1.3.3 Fuses

Two fuses and a thermostat protect the instrument. The fuses are installed in bayonette fuse holders mounted on the rear panel. Both sides of the AC power line are fused. Slo-blo 1.5 AMP fuses are recommended for 105-130 volt operation and slo-blo 0.75 AMP for 210-225 volt operation. The thermostat is mounted on a metal bracket with the series regulator transistor and several filter capacitors and is wired in series with the AC power line and the power transformer primary. It is designed to open when the temperature of the mounting bracket rises to 180° ± 5°F, and close when the temperature falls below 140° ± 8°F.

1.4 SPECIFICATIONS

1.4.1 Specifications for DC Voltage Measurements

Ranges:

Ranges F.S.	100MV	1000MV	10V	100V	750V
Overrange (0.1 Sec. Sample)	120.00MV	1200.00MV	12.000V	120.00V	750.0V
Overrange (1.0 Sec. Sample)	*120.000	*1200.00	*12.0000	*120.000	750.00
Input Resistance	110K	1.1 Meg	11 Meg	10 Meg	10 Meg

Accuracy Under ASA Reference Conditions (23°C ± 1°)

0.1 Second Sample: .01% of full scale ± .01% of reading on all ranges

1.0 Second Sample: .01% of full scale ±.01% of reading on 100MV F.S. range;
.005% of full scale ± .01% of reading on 1000MV F.S. range;
.002% of full scale ± .01% of reading on 10V F.S. range;
.001% of full scale ±.01% of reading on 100V F.S. range;
.001% of full scale ± .01% of reading on 750V F.S. range.

Table 1.2. Connector J101 Terminal Information

PIN		FUNCTION
B	0	
F	1	
L	2	
R	3	
V	4	10^0 Digit of Measurement
Z	5	
d	6	
j	7	
p	8	
u	9	
y		
CC		
HH		
D	0	
J	1	
N	2	
T	3	
X	4	
b	5	10^1 Digit of Measurement
f	6	
m	7	
s	8	
w	9	
AA		
EE		
A	0	
E	1	
K	2	
P	3	
U	4	
Y	5	10^2 Digit of Measurement
c	6	
h	7	
n	8	
t	9	
x		
BB		
FF		
C	0	
H	1	
M	2	
S	3	
W	4	
a	5	10^3 Digit of Measurement
e	6	
k	7	
r	8	
v	9	
z		
DD		

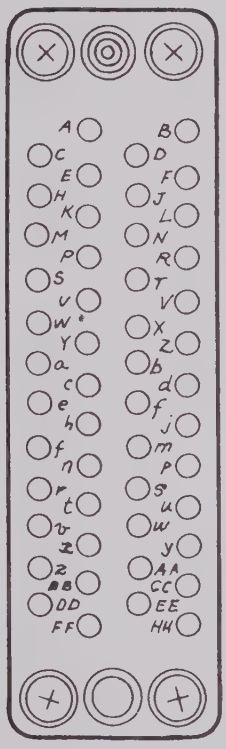
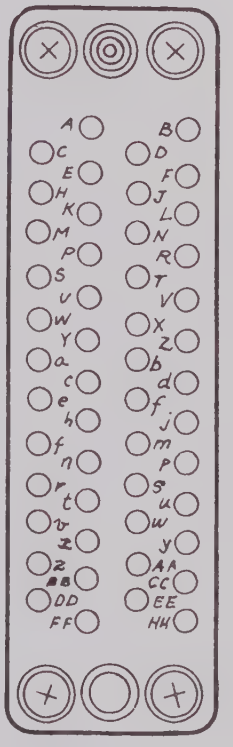


Table 1.3. Connector J102 Terminal Information

PIN		FUNCTION
B	0	10^4 Digit of Measurement
F	1	
L	2	
R	3	
V	4	
Z	5	
d	6	
j	7	
p	8	
u	9	
y		
CC		
HH		
D		
J	1	(XXXX. X Range Code)
N	2	(XXX. XX Range Code)
T	3	(XX. XXX Range Code)
X	4	(X. XXXX Range Code)
b	5	(. XXXXX Range Code)
f	6	(. 0XXXXX Range Code)
		volts, milliseconds, or kilocycles
m		
s		
w		
AA		
EE		
A		
E	E	(Overrange Symbol)
K	+	(Positive DC Voltage Mode Symbol)
P	-	(Negative DC Voltage Mode Symbol)
U		
Y	KC	(Frequency Mode Symbol)
c		
h		
n		
t	MS	(Period or Time Interval Mode Symbol)
x		
BB		
FF		
C		
H		
M		
S		
W		
a		
e		
k		Print Command
r		
v		
z		Encode Command
DD		Logic Ground



Accuracy Under ASA Rated Conditions: (12°C to 40°C)	.03% of full scale ± .03% of reading on 100 MV F.S. range; .015% of full scale ± .03% of reading on all other ranges
Polarity:	Automatic, + or -
Sample Period:	0.1 second or 1.0 second
Encode Interval:	Fixed: 0.11 second and 1.01 second Variable: 0.2 to 5 seconds Single: as commanded
Common Mode Interference Rejection:	140 db minimum at DC 120 db minimum at 60 cps, with up to 1K ohm unbalance
Chassis to LO Terminal Capacitance:	2.6 pfd maximum
Common Mode Voltage Limit:	750 volts peak without damage 500 volts peak, guard to LO terminal
Normal Mode Interference Rejection When Using 0.1 Second Sample	**Infinite at frequencies evenly divisible by 10 (e.g., 10, 20, 30, 40 cps, etc.)
Normal Mode Interference Rejection When Using 1-Second Sample:	**Infinite at frequencies evenly divisible by 1 (e.g.., 60, 61, 62, 63 cps, etc.)

* Most significant digit (1) is not displayed but is indicated by symbol "E" display when overrange condition occurs.

** For other frequencies refer to figures 1.1 and 1.2.

1.4.2 Specifications for Frequency Measurements

Frequency Range:	10 cps to 1 megacycle
Selectable Ranges:	999.99 kcs F.S. with 20% overrange capability 99.999 kcs F.S. with 20% overrange capability 9.9999 kcs F.S. with 20% overrange capability
Resolution:	0.0001 kcs
Accuracy:	.01% of reading ± 1 count

Input Signal Level Requirement:	300 mv P-P to 50V P-P
Input Impedance:	1 megohm shunted by 50 pf

1.4.3 Specifications for Period or Time Interval Measurements

Frequency Range	
Period Measurements:	*0.1 cps to 100 cps
Interval Measurements:	*0.05 cps to 50 cps
Selectable Ranges:	99.999 milliseconds F.S. with 20% overrange capability 999.99 milliseconds F.S with 20% overrange capability 9999.9 milliseconds F.S. with 20% overrange capability
Accuracy:	.01% of reading ± 1 count
Input Signal Level Requirement:	**300mv P-P (for signals having rise times of 200mv/millisecond, or greater) to 50V P-P

* Increase minimum signal level required by 20 db/decade for frequencies to 5kc on period measurements and 2.5kc on interval measurements.

** Increase minimum signal level required by 20 db/decade for signals having slower rise times (i.e., 10 cps sine wave requires 3V P-P).

1.4.4 Miscellaneous Specifications

Electrical Outputs:

Measurement:	5 digits in 10-line decimal: true = 0 volt at 1 milliampere; false = +50 to +70 volts at 100 microampere maximum load.
Range Symbol:	6 lines: true = 0 volts at 1 milliampere; false = +50 to +70 volts at 100 microamperes maximum load (see Table 1.3).
Polarity, Overrange,	5 lines: true = 0 volts at 1 milliampere; false = +50 to +70 volts at 100 microamperes maximum load (see Table 1.3).
Print Command:	12-volt pulse, positive going from ground, with 1 microsecond rise time.

Electrical Inputs:	
Encode Command:	Closure between pins z and DD of J102, or negative-going waveform at pin z of J102 from +8 to +12V to ground with a fall time of 1μsecond.
AC Power Requirement:	105-130 volts, 50-400 cps, single phase (210-235 volts, 50 to 400 cps, single phase, when so modified).
Case Dimensions:	5-1/4" high x 20-3/4" deep x 17" wide.
Net Weight:	36 lbs.
Shipping Weight:	56 lbs. (approximately)

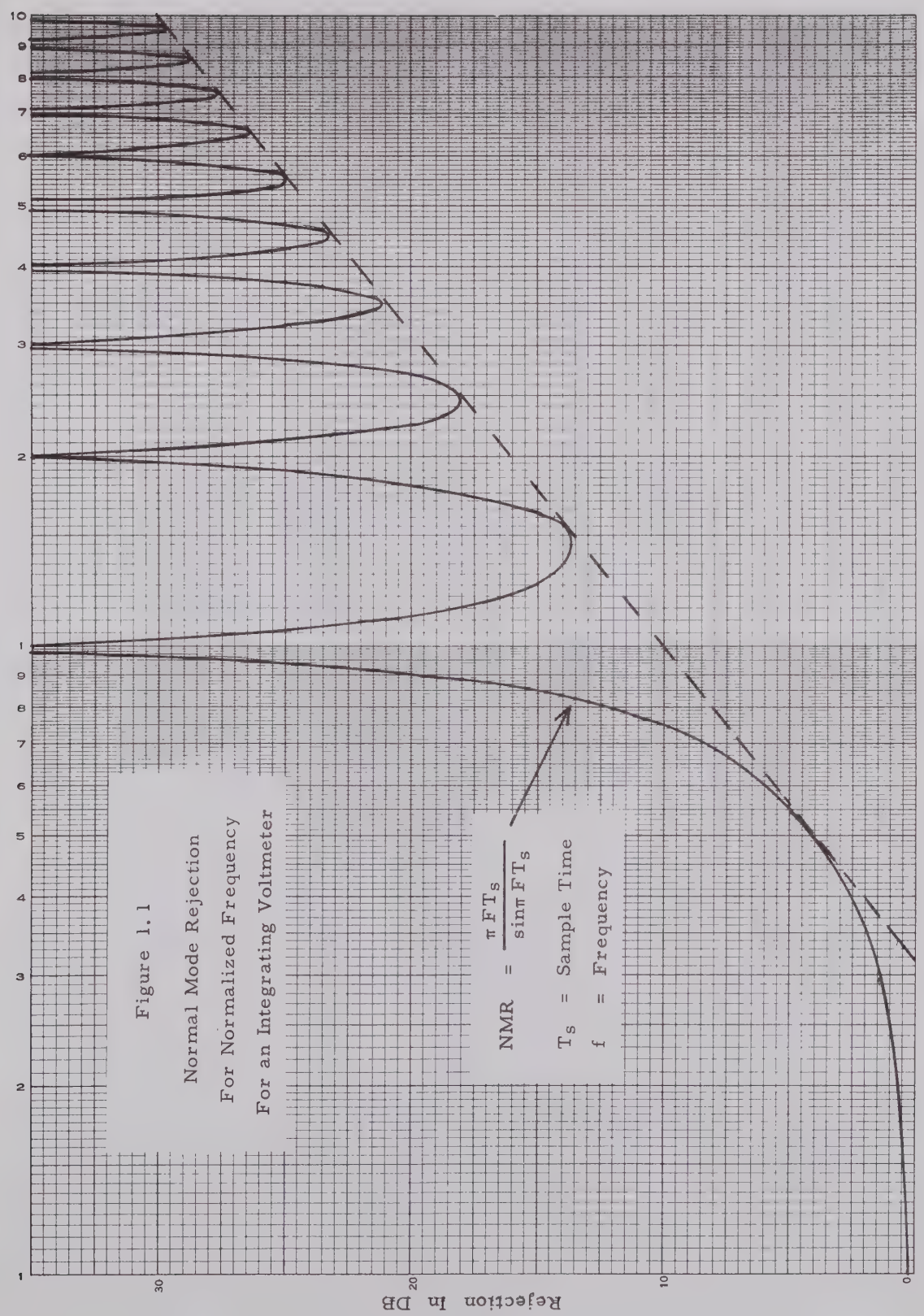


Figure 1.1

Normal Mode Rejection
For Normalized Frequency
For an Integrating Voltmeter

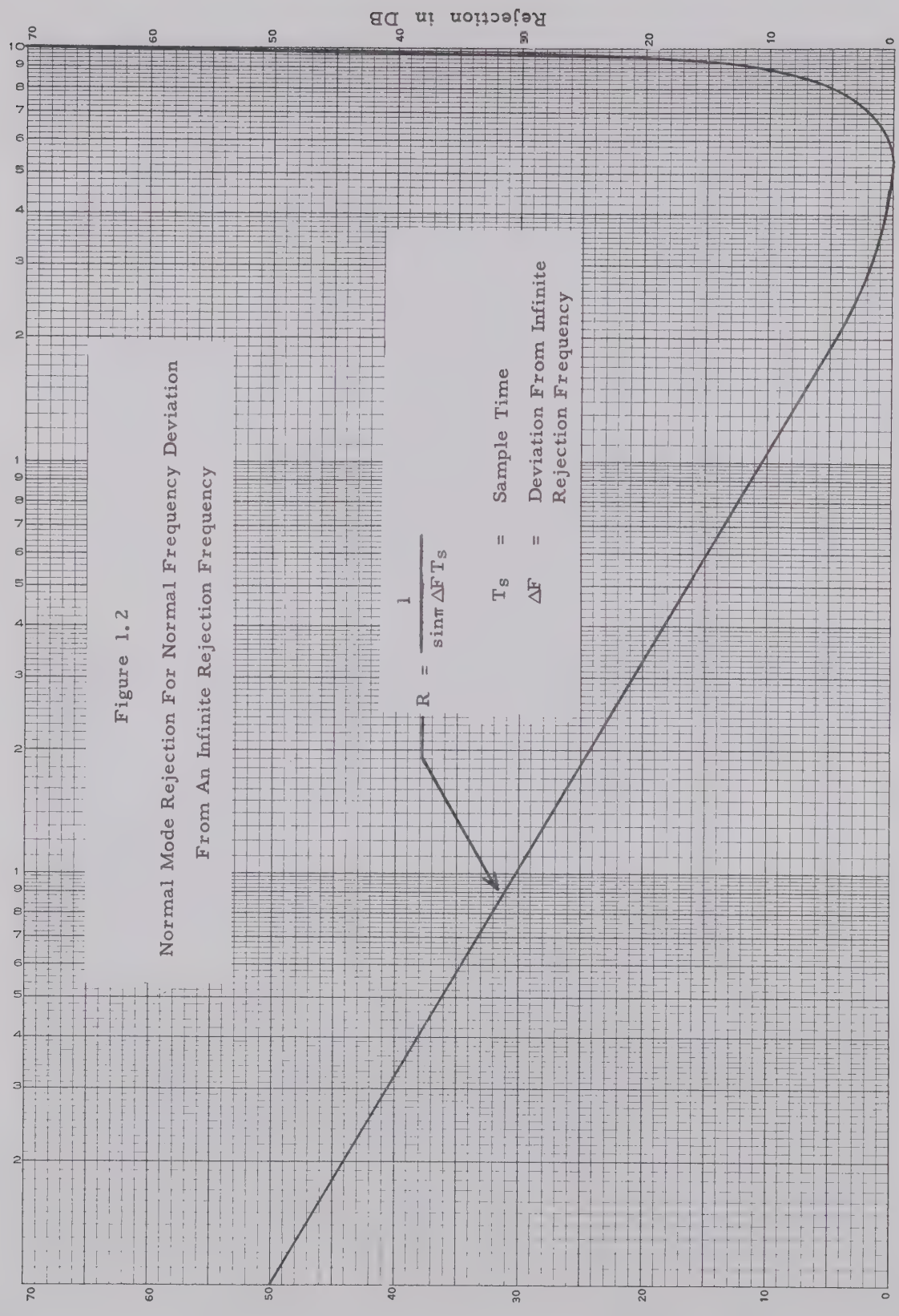


Figure 1.2

Normal Mode Rejection For Normal Frequency Deviation From An Infinite Rejection Frequency

SECTION II

OPERATION

2.1 INSPECTION

After the instrument is unpacked it should be inspected for shipping damage. If damage is found an immediate report should be made to the shipping agency and to Electro Instruments, Inc. If equipment fails to operate as specified, check all connectors, cables, and fuses, and ensure that all plug-in circuit boards are firmly seated. Should the equipment fail to operate satisfactorily during the warranty period follow the procedure outlined in the warranty page of this manual.

2.2 INSTALLATION

The Model 630 is delivered from the factory ready for installation in a standard 19 inch panel rack. For bench use it may be desirable to remove the rack mounting brackets attached to either side of the case. The unit should be mounted in a manner which will not restrict air flow through it.

2.3 AC POWER INPUT

Each instrument is supplied with an AC power cable and is delivered from the factory ready to operate from a 3-terminal 105-130 volt, 50-400 cps power source. Modifications to the power supply and AC regulator board 104-104, as shown in figure 2.1, will permit the instrument to be used with 210-225 volt AC power source.

CAUTION

Line voltage surges should never be allowed to exceed 145 volts for 105-130 volt operation, or 240 volts for 220 volt operation. Peak voltages greater than these may damage the power supply series regulator.

NOTE

For 105-125 volt operation the two fuses at the rear of the instrument should be 1.5 Amp. Slo-Blo type. For 210-235 volt operation the fuses should be reduced to 0.75 Amp Slo-Blo.

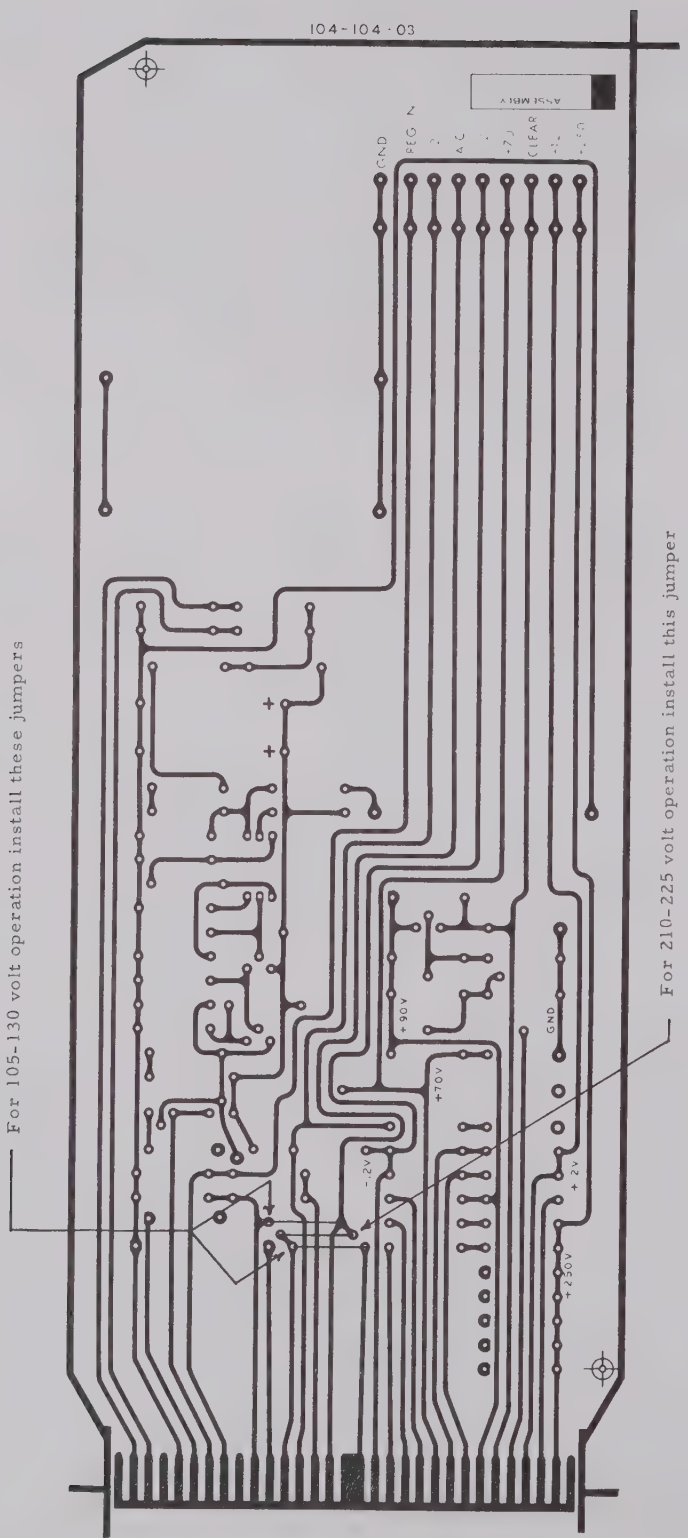


Figure 2.1. Modifications Required on AC Power and Regulator Board 104-104 for 210-225 Volt Operation

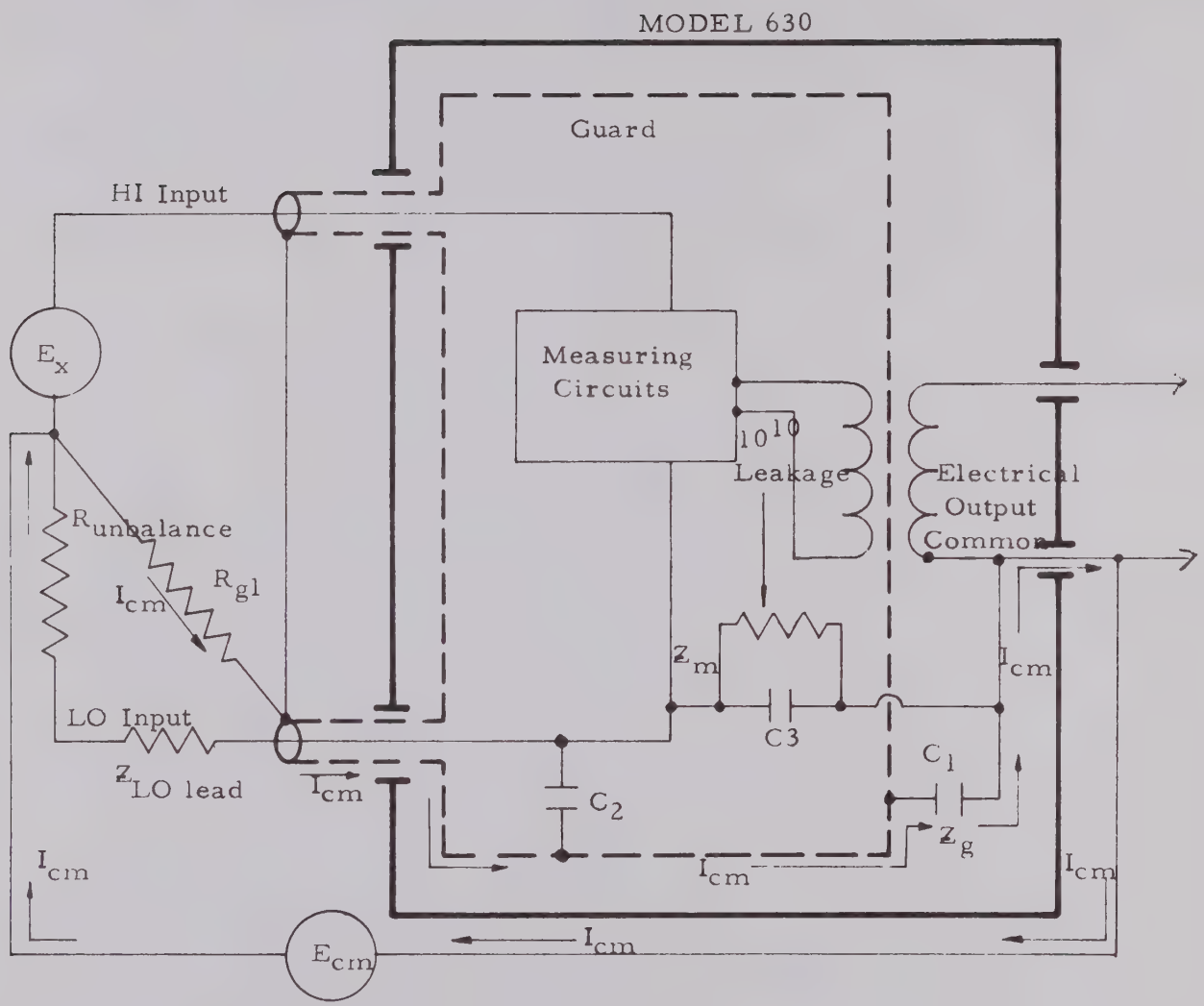
2.4 SIGNAL INPUT AND GROUNDING CONSIDERATIONS

When connecting signal sources to the Model 630 consideration should be given to the isolation capability provided by the guard circuit, a special feature incorporated in this instrument. Guarding is illustrated in figure 2.2. It is utilized to reduce the ill-effects that common mode voltages have upon the normal mode measurements. Guarding is not another name for shielding. It is an entirely different technique which works in two ways: it surrounds the measurement leads and circuitry with a potential shield, and it supplies an alternate path for common mode currents so that they do not flow through $R_{unbalance}$ or along the instrument leads.

The potential shield function involves holding the guard at exactly the same potential as the measuring circuits in order that all currents are effectively blocked from flowing between the two. The guard consists of a highly insulated conducting metal shield within the meter, completely surrounding the measuring circuits and the input leads. It is also connected to a guard lead which is brought out of the meter as a separate conductor. By connecting the guard lead to the source of common mode voltage, the guard is driven to the same potential as the common mode voltage source, which is unavoidably present on the leads and the measuring circuits. With the guard held at the E_{cm} potential no potential difference can exist and no current will flow since $I = \frac{E}{R}$. Therefore, the flow of common mode currents is effectively blocked from the measuring leads and circuits and flows harmlessly along the guard lead to the guard, returning to its source via the impedance Z_g (approximately 330pf) between guard and electrical output common.

The capacitance C_2 (approximately 3000pf) existing between the guard and the measuring circuits is never charged or discharged because both are held at the same potential. This results in an effective capacitance between the measuring circuits and the electrical output common terminal of approximately 2.5pf. As it is shunted by the leakage resistance (approximately 10^{10} ohms) from the measuring circuits to ground this guarded capacitance becomes Z_m, the guarded impedance (approximately 10^9 ohms at 60 cps). This high value of Z_m effectively blocks any appreciable I_{cm} current from flowing in the measurement leads. No disturbing E_{cm} voltages are therefore developed across the series impedance of the leads or across $R_{unbalance}$. Thus E_{cm} cannot materially affect E_x.

If the common mode voltage is common to one of the measurement terminals the LO side and the GUARD should be connected as shown in figure 2.3. For frequency measurements the GUARD should always be connected to the low side of the signal source as shown in figure 2.4.



C_1 = Guard/electrical-output-common capacitance ≈ 3300pf.
C_2 = Guard/measuring circuit capacitance (≈ 3000pf ACTUAL).
C_3 = Measuring circuits/electrical outputs common capacitance (2.5pf effective) = guarded capacitance.
Z_g = Impedance, guard to electrical outputs common.
Z_m = Effective impedance, measuring circuits to electrical outputs common.

Figure 2.2. Guard Circuit

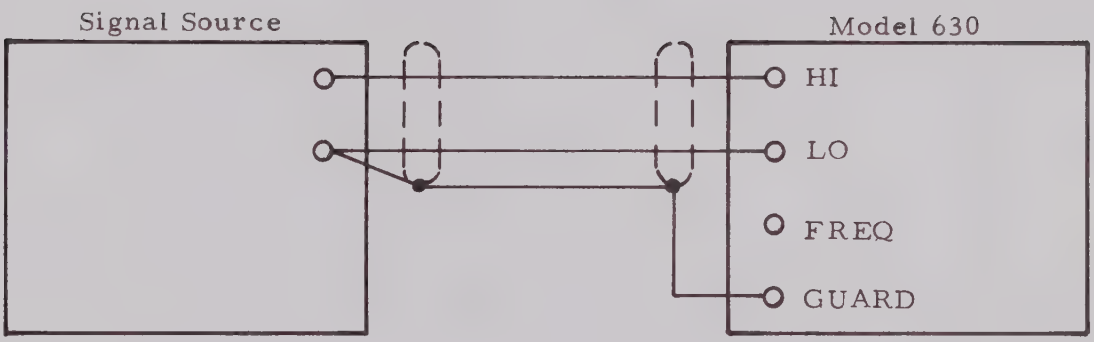


Figure 2.3. Signal Input Connections for DC Voltage, Time Interval, or Period Measurements when Common Mode Voltage is common to one of the Measurement Terminals.

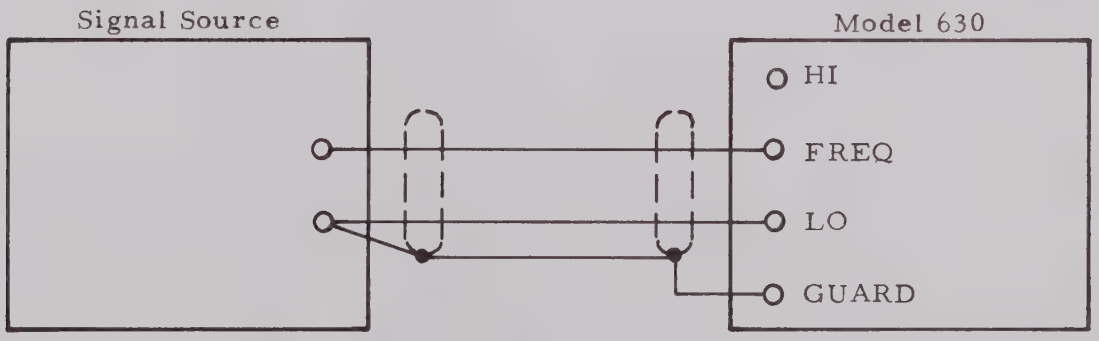


Figure 2.4. Signal Input Connections for Frequency Measurements

2.5 OPERATING PROCEDURE FOR DC VOLTAGE MEASUREMENTS

a. Connect power cable to appropriate AC power source (see paragraph 2.3).

b. Set POWER switch to ON. Allow 15 minutes for warmup.

c. Using the FUNCTION switch and the RANGE switch, select DC volts measuring mode and appropriate range in accordance with table 2.1.

Table 2.1. Function Switch and Range Switch Settings for DC Voltage Measurements

RANGE	SAMPLE PERIOD SETTING ON FUNCTION SWITCH	RANGE SWITCH SETTING
000.01 to 120.00 millivolts	.1 sec	100MV
0000.1 to 1200.0 millivolts	.1 sec	1000MV
00.001 to 12.000 volts	.1 sec	10V
000.01 to 120.00 volts	.1 sec	100V
0000.1 to 0750.0 volts	.1 sec	750V
00.001 to 120.000 millivolts	.1 sec	100MV
000.01 to 1200.00 millivolts	1 sec	1000MV
0.0001 to 12.0000 volts	1 sec	10V
00.001 to 120.000 volts	1 sec	100V
000.01 to 750.00 volts	1 sec	750V

d. Connect signal cable to HI, LO, and GUARD terminals at rear rail. (Refer to paragraph 2.4)

WARNING

With signal leads connected to the meter, any common mode voltage existing between the signal source and ground will also be present between the guard housing, inside circuitry, and earth ground. This presents no hazard as long as the

front service door is closed and the guard shield is kept well insulated. Before the front door is opened disconnect the signal leads from the meter or confirm that no hazardous common-mode voltages exist at the signal source.

e. Set ENCODE switch to one of the following positions:

(1) Set to CONT for repetitive encodings at maximum rate, or

(2) Set to VAR for repetitive encodings with the time intervals between encodings adjustable with the variable control between 0.2 and 5 seconds, or

(3) Set to REMOTE if encodings are to be initiated manually or by remote control.

f. If encodings are to be initiated manually, momentarily rotate ENCODE switch to SINGLE position to start each encoding. If encodings are to be initiated by remote control apply momentary contact closure between terminals z and DD of connector J102 to start each encoding. If the ENCODE switch has been set at CONT repetitive encodings will occur automatically at intervals of 1.5 milliseconds after the end of a sample period. If the ENCODE switch has been set at VAR repetitive encodings will take place automatically at intervals between 0.2 and 5 seconds, as determined by the setting of the variable ENCODE control.

2.6 OPERATING PROCEDURES FOR FREQUENCY MEASUREMENTS

a. After instrument has been connected to suitable AC power source as explained in paragraph 2.3, set POWER switch to ON. Allow 15 minutes for warmup.

b. Select with the FUNCTION switch the frequency measuring mode and appropriate range as indicated in table 2.2.

Table 2.2. Function Switch Time Base Settings for Frequency Measurements

RANGE FULL SCALE	SWITCH SETTING
999.99 kcs	.1 SEC SAMPLE
99.999 kcs	1 SEC SAMPLE
9.9999 kcs	10 SEC SAMPLE

c. Connect Signal cable to FREQ, LO, and GUARD input jacks on rear panel as explained in paragraph 2.4.

WARNING

With signal leads connected to the meter, any common mode voltage existing between the signal source and ground will also be present between the guard housing, inside circuitry, and earth ground. This presents no hazard as long as the front service door is closed and the guard shield is kept well insulated. Before the front door is opened disconnect the signal leads from the meter, or confirm that no hazardous common mode voltages exist at the signal source.

d. Set ENCODE switch as in steps e and f of paragraph 2.5.

2.7 OPERATING PROCEDURES FOR PERIOD OR TIME INTERVAL MEASUREMENTS

a. After instrument has been connected to suitable AC power source as explained in paragraph 2.3, set POWER switch to ON. Allow 15 minutes for warmup.

b. Select with the FUNCTION switch the period/time interval measuring mode and appropriate range in accordance with table 2.3.

Table 2.3. Function Switch Settings for Period or Time Interval Measurements

RANGE	SWITCH SETTING
00.001 to 99.999 milliseconds	PERIOD-INTERVAL .1 SEC
000.01 to 999.99 milliseconds	PERIOD-INTERVAL 1 SEC
0000.1 to 9999.9 milliseconds	PERIOD-INTERVAL 10 SEC

c. Connect signal cable to HI, LO, and GUARD input jacks at rear rail, as illustrated in figure 2.2.

WARNING

With signal leads connected to the meter, any common mode voltage existing between the signal source and ground will also be present

between the guard housing, inside circuitry, and earth ground. This presents no hazard as long as the front service door is closed and the guard shield is kept well insulated. Before the front door is opened disconnect the signal leads from the meter, or confirm that no hazardous common-mode voltages exist at the signal source.

d. Using table 2.4 and figure 2.5 as guides, select with SLOPE switch that portion of input waveform on which measurement will start and on which measurement will stop. (Starting and stopping times apply to the slope of the waveform as it passes through the zero axis in the positive or negative direction.)

Table 2.4. Slope Switch Settings for Period and Time Interval Measurements

SWITCH SETTING	COUNTING INTERVAL
-/-	Starts on Negative Slope, Stops on Negative Slope
+/+	Starts on Positive Slope, Stops on Positive Slope
-/+	Starts on Negative Slope, Stops on Positive Slope
+/-	Starts on Positive Slope, Stops on Negative Slope

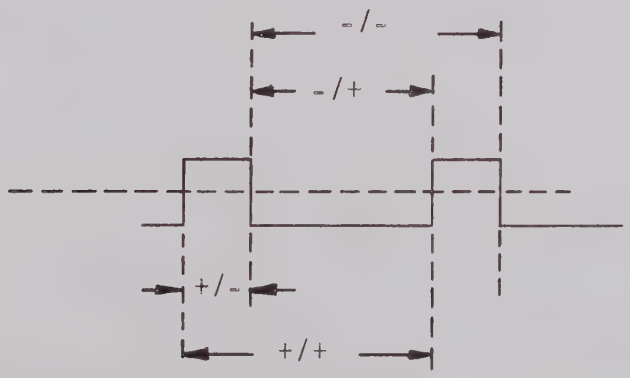


Figure 2.5. Period or Time Intervals Selected With SLOPE Control

NOTE

Figure 2.5 shows the time that will be measured by the Model 630 with the SLOPE switch in the various positions. Normally, +/+ and -/- will result in the same time unless the waveform has a relatively slow rise time on one slope. For best accuracy the steepest slopes of the waveform should be selected.+/+ and -/- result in a period measurement that is the time for one complete cycle. The -/+ and +/- positions allow measurement of each half of the cycle. In most cases +/- time plus the -/+ time will equal the +/+ or -/- time.

e. Set ENCODE switch to VAR and rotate the variable ENCODE control to its fully clockwise position. (Continuous encode mode should not be used.)

2.8 OPERATION WITH DIGITAL PRINTER OR SCANNER

Electrical in-line signals provided at connectors J101 and J102 can be used to directly drive an Electro Instruments Model 9057 Digital Printer, or similar output device requiring 0 volts on selected lines and +70 volts on non-selected lines. The combination can also be expanded to include a scanner such as Electro Instruments Model 707A-120 or 707A-600. When operating with the printer as shown in figure 2.6 the combination functions as a closed loop system: the Model 630 commands the printer to print; after printing, the printer produces a print complete signal which commands the Model 630 to encode the next measurement. Figure 2.7 shows the scanner as part of the closed loop. Here the scanner commands the meter to encode and the meter commands the printer to record the measurement. At completion of the print cycle the printer commands the scanner to step to the next channel.

The print command provided by the Model 630 is a 12 volt pulse, positive-going from ground with a rise time of one microsecond. Information provided at J101 and J102 includes five 10-line decimal digits representing measurement magnitude, seven range codes, one over-range symbol (E), and four operating mode symbols (+, -, KC, MS).

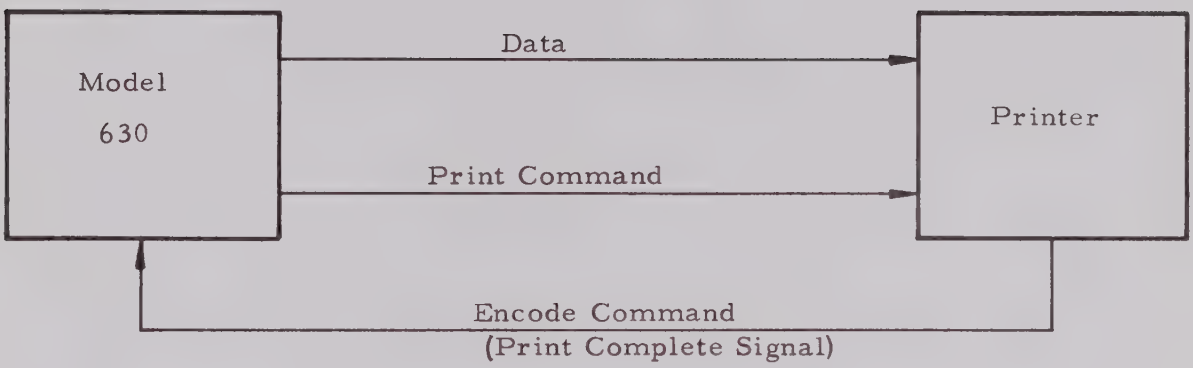


Figure 2.6. Model 630 Operating with Digital Printer

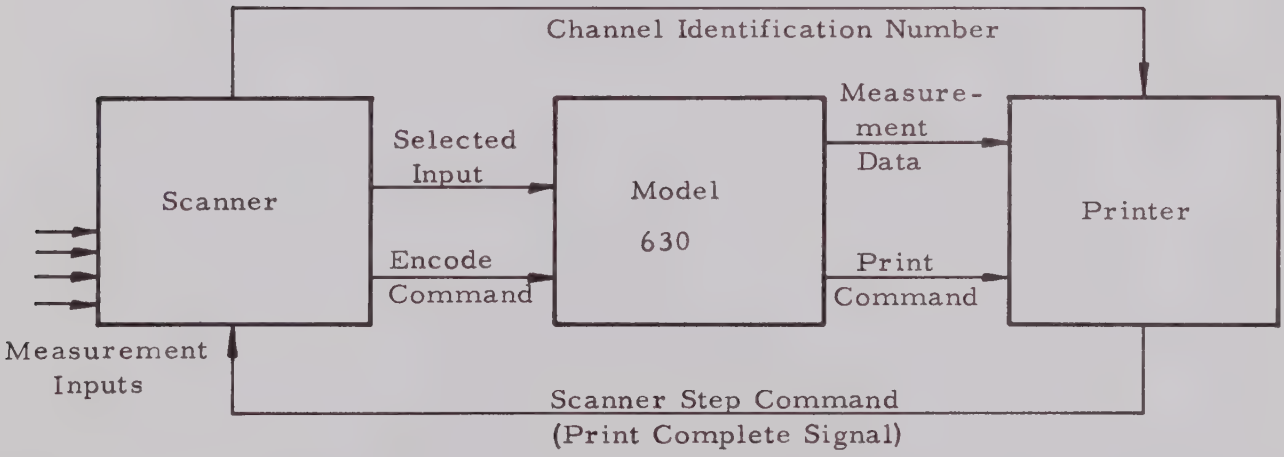


Figure 2.7. Model 630 Operating with Scanner and Digital Printer

SECTION III

THEORY OF OPERATION

3.1 GENERAL

The Model 630 measures DC voltage, frequency, period, and time interval. The FUNCTION switch selects the type of measurement and time base, and a RANGE switch selects the attenuation factor on DC voltage and period measurements. The ENCODE switch selects the sampling rate, and a SLOPE switch selects the slope of the input waveform on which period or time interval measurements will start and stop.

The method for accomplishing the measurements is discussed in the following paragraphs. In the discussion the reader should refer to the overall block diagram and the appropriate schematics.

The logic circuits and symbology supplement following section V explains the logic circuits used in the instrument and the symbols used in this manual to represent these circuits.

3.2 DEFINITIONS OF TERMS USED IN TEXT

In the following discussion, sampling period is that portion of the encoding time during which the meter senses the input signal and accumulates information. The display and storage cycle interval is that portion of encoding time immediately following the sampling interval during which the meter evaluates the information accumulated and produces a visual display. Encoding time is defined as the total time required for the meter to produce a visual display after a sample command is first applied.

3.3 DC VOLTAGE MODE

DC voltage measurements are accomplished by the Model 630 using a DC to frequency conversion principle. After first passing through the range attenuator network, the signal being measured (E_x) is converted to a train of sawtooth waves. The sawtooth waves are produced by a closed loop system consisting of a precision pulse former and a combination integrating-operational amplifier which is highly stabilized (see figure 3.1). The sawtooth waveform frequency is directly related to the measured signal. The average amplitude of the wavetrain determines the operating frequency of a voltage controlled oscillator (VCO) having a center frequency of 200 KCS and a normal operating range between 100 KCS and 300 KCS. Negative values of E_x cause a proportionate decrease

in the oscillator frequency below 200 KCS, and positive values of E_x increase the frequency proportionately above 200 KCS. Since the VCO, pulse generator, and integrator amplifier are in a closed loop system, and the amplifier has very high gain, the accuracy linearity and stability of the voltage to frequency conversion is largely determined by the width and height determining portion of the pulse generator, and is independent of the stability and linearity of the VCO.

The number of pulses generated by the VCO during the fixed time base period are totalled by a 5-decade binary counter (paragraph 3.6) which is preset to display 00000 volts for the 200 KC condition. At the end of the counting interval the accumulated count (for positive voltage measurements) or the nines complement of the accumulated count (for negative voltage measurements), is converted from binary code to decimal and displayed.

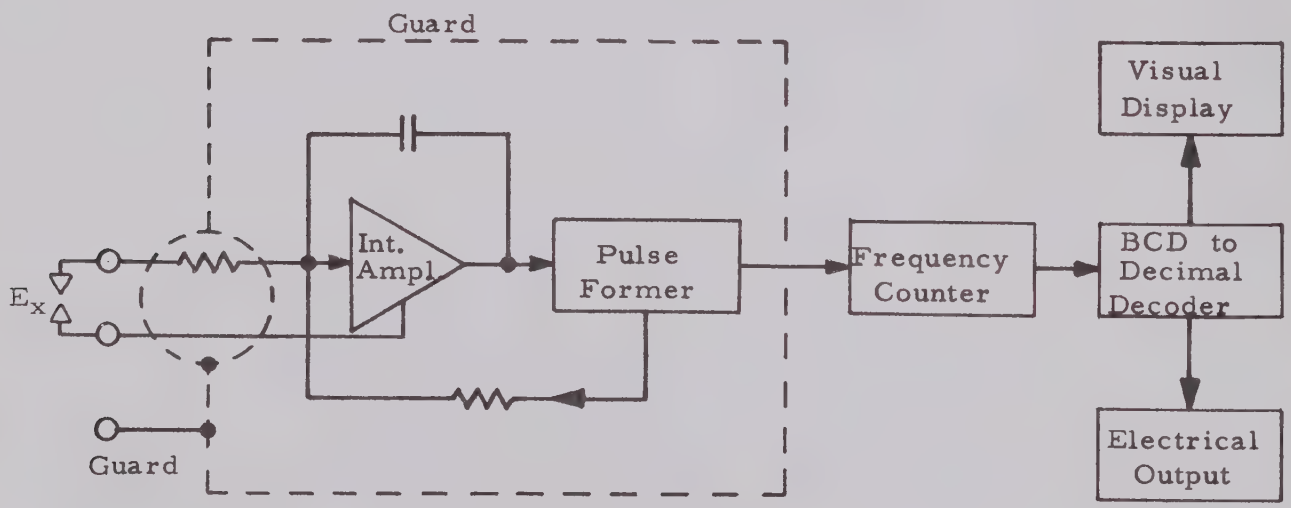


Figure 3.1. Model 630 Simplified Block Diagram

3.3.1 Range Attenuator Switch

The RANGE switch, S2, a ganged 5-position, 6-section switch, connects various combinations of voltage divider networks into the measuring input circuit whenever the meter is in the DC volts or period/time interval mode. For the DC volts mode, these networks attenuate the input signal E_x in five full-scale decade steps: 0.1 volt, 1 volt, 10 volts, 100 volts, and 750 volts. For period/time interval operation the 1 volt position is the recommended switch setting, in which range the meter will operate normally for input voltages within the range of 300 millivolts to 50 volts peak-to-peak. The attenuator circuit is shown in figure 3.2. For all ranges, associated divider networks are proportioned to maintain a 100 millivolt level at the junction of R18 and R127 for full scale input.

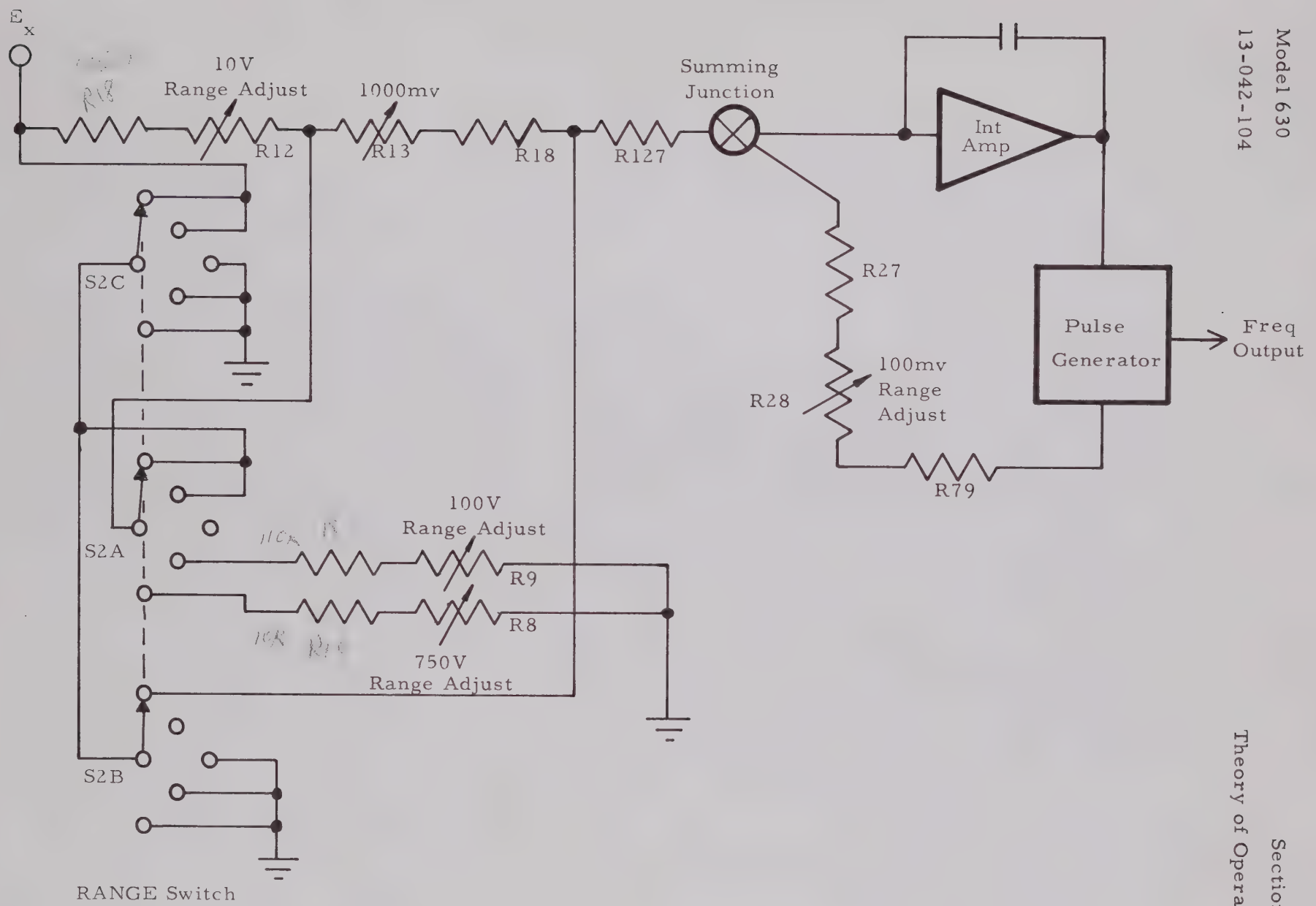


Figure 3.2. Range Switching Network

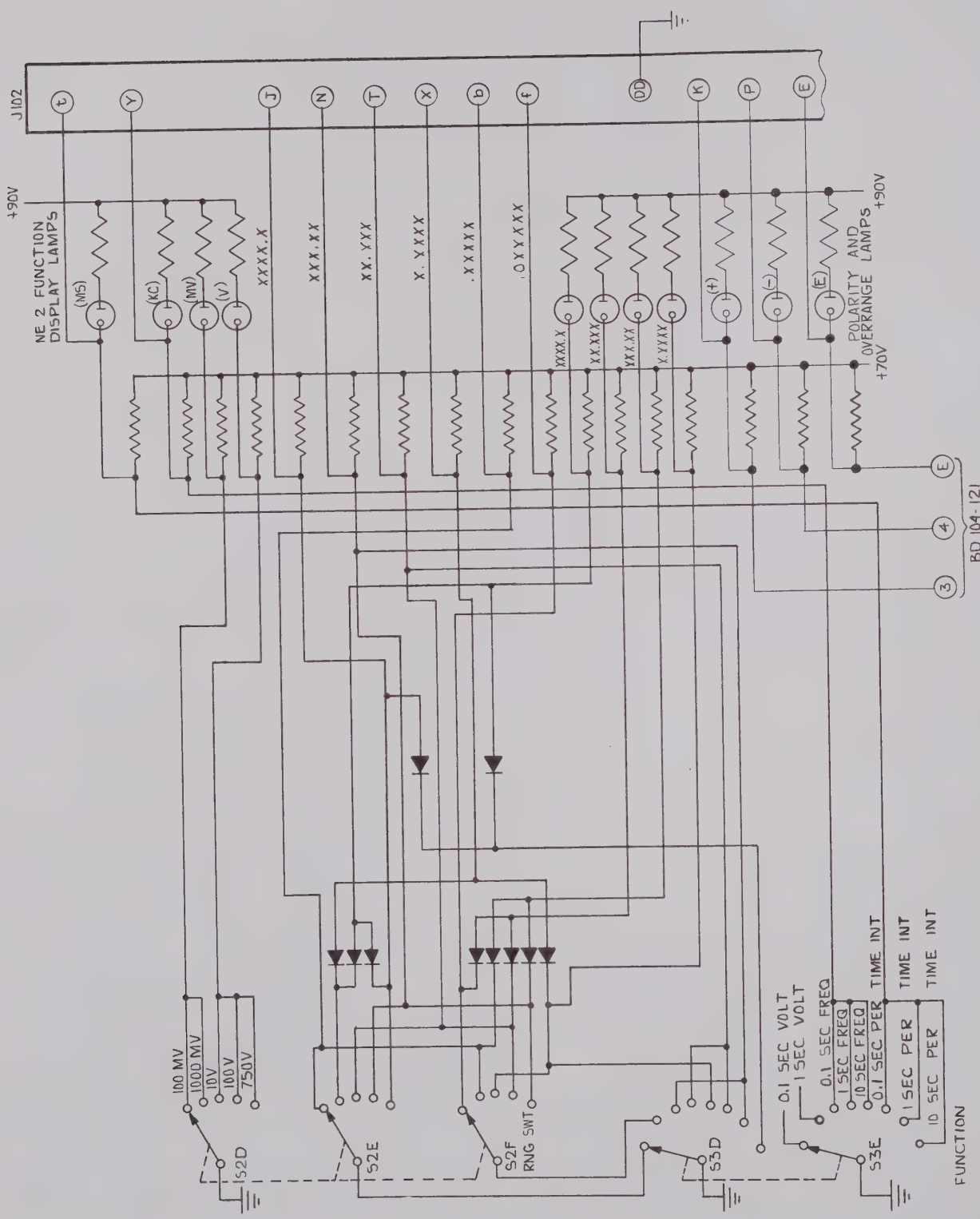


Figure 3-3. Decimal Point and Symbol Lamp Control

3.3.1 Range Attenuator Switch (Continued)

R28 is the 100 millivolt range calibration control and its setting fixes the voltage to frequency conversion factor of the operational amplifier and associated feedback circuits (refer to paragraph 3.3) from the junction of R18 and R127 to the output of the VCO (TP3) at 1 MC per volt. This adjustment must be set before the other ranges can be calibrated. The voltage to frequency conversion factor is 100 KC per volt. R13 is the calibration control for the 1 volt range, R12 for the 10 volt range, R9 for the 100 volt range, and R8 for the 750 volt range. Sections D, E, and F of the RANGE switch are used in conjunction with the FUNCTION switch to select and energize the decimal point and operating mode indicator lamps on the front panel. The voltage levels used to energize these lamps are also the same signals provided at output connector J102 to represent these functions in the electrical output format. (See figure 3.3.)

3.3.2 DC to Frequency Converter

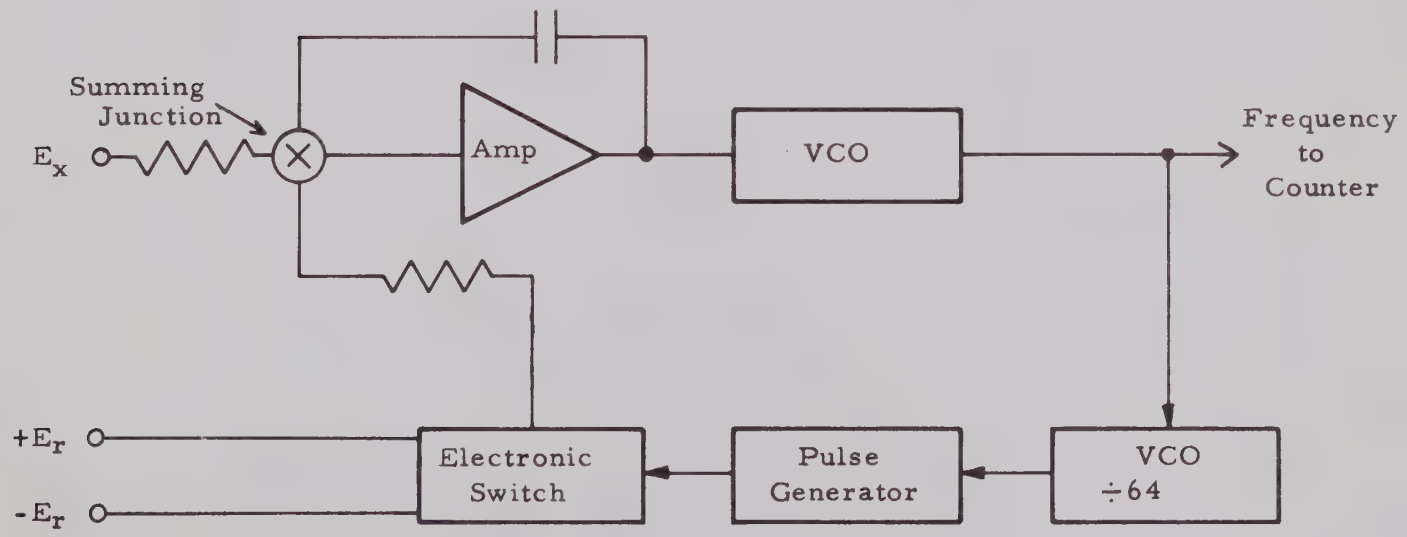


Figure 3.4. DC to Frequency Converter

The DC to frequency converter can be broken down into four blocks as shown in figure 3.4. These are:

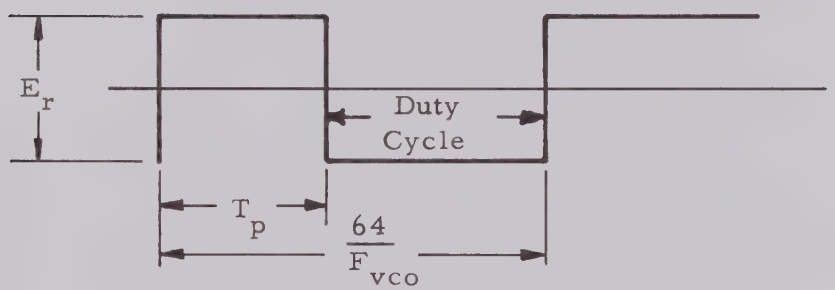
a. Integrating amplifier

b. Voltage controlled oscillator (VCO)

c. Pulse generator

d. Electronic switch and precision reference voltage supply.

Connected together, these four blocks form an operational system. The unknown input voltage E_x is applied through resistor networks such that one (least significant) digit is represented by a current flow of 10^{-11} ampere on a 1-second sample into a summing junction. This junction is at the input of a DC wide-band amplifier having a DC voltage gain factor in excess of 10^7. The input current to the summing junction flows through R127, depending on the RANGE. Output from the DC wide-band amplifier is applied to a voltage controlled oscillator (VCO) whose frequency of oscillation is determined by the average level of the voltage applied. It is the output frequency of this oscillator which is counted by the display counters. The VCO pulses are also fed to a frequency divider which is located on the inside power supply board. This divider produces one pulse for every 64 VCO pulses in. The output of the VCO divider controls, by means of a precision pulse generator, an electronic switch having an output frequency identical to that of the VCO divider output and a duty cycle proportional to the divider output frequency. This can be seen in figure 3.5.



$$\bar{E} = E_r \frac{T_p}{64/F_{vco}} = \frac{F_{vco} E_r T_p}{64}$$

E_r is the reference voltage

$\bar{E}$ is the average voltage out of the precision switch (referenced to the minus side of E_r)

T_p is the fixed pulse width

F_{vco} is the VCO frequency (the factor 64 results from dividing the VCO frequency by 64)

Figure 3.5. Electronic Switch Output Waveform

The voltage from the precision switch is applied through R27 to the summing junction. This signal represents negative feedback since an increasing current into the summing junction will drive the VCO to a lower frequency, which will have the effect of reducing the current flow through R27.

When operating normally, the accuracy, stability, and linearity of the system in converting the unknown voltage to a frequency is determined by the stability of the input attenuator R8, R9, R12, R13, and R127 with associated trim resistors, the reference voltage E_r, and the fixed pulse width time T_p.

3.3.3 Integrator Amplifier Operation

This amplifier is of the common two-channel type. The DC portion of the summing junction signal is taken off through R26 and R1 to the input of a chopper-type amplifier. The AC portion of the summing junction signal is applied through a capacitor C10 to the grid of nuvistor V2. By splitting the AC and DC signal in this manner, it is possible to obtain the low drift of a chopper type amplifier and at the same time, the large bandwidth of a direct coupled amplifier. The paths that the signals take can be seen by referring to the integrator amplifier schematic.

DC Channel: The DC summing junction voltage appears at the junction of R1 and C1 when the chopper is open between pins 3 and 4. When these contacts close the junction of R1 and C1 falls nearly to zero volts, and an AC signal appears on the grid of V1. This signal increases in peak-to-peak value as the magnitude of the DC on the summing junction increases. This signal is now amplified by V1, Q1, Q3, Q4, Q5, Q6, and Q7 and applied through capacitor C21 to a demodulator.

The contact between pins 1 and 7 of the chopper is used to demodulate the amplified signal back to pulsating DC which is then applied through R53 to an active filter made up of Q16, Q17, and C13. The filter removes ripple caused by the modulation/demodulation process.

The chopper amplifier is directly coupled (except for input and output capacitors); thus, it is necessary to stabilize (set) the operating point of the input stage (V1) to avoid driving Q7 outside its dynamic range. This is accomplished by using a DC feedback loop formed by R56, C17, R6, etc., to reduce the DC gain inside the demodulator and modulator to near unity. The AC gain between the grid of V1 and the emitter of Q7 is negative (inverting); however, it should be noted that the DC to DC gain from the summing junction to the base of Q17 is positive (non-inverting) due to the additional inversion caused by the modulation

demodulation process. Active filter Q16, Q17, provides another inversion before the amplified DC signal is fed into the cathode of V2 in the wideband amplifier.

3.3.3.1 Wide Band Channel:

AC signals from the summing junction are applied through C10 to the grid of nuvistor V2. The amplified DC signal from the chopper amplifier is applied to the cathode of V2 in such a phase relationship that the signal on the plate of V2 is proportional to the sum of the AC and DC components. The signal at the plate of V2 is applied to a series of direct coupled stages consisting of Q18, Q19, Q20, Q21, and Q22. These stages carry all frequency components of the signal.

3.3.3.2 Limiters and Rolloffs:

Several stages in both the wideband and DC channels have limiters which set the maximum base current of a stage. For example, consider the limiter at the base of Q21. If transistor Q20 is driven hard, its collector becomes positive. The base of Q21 will normally be about 0.6 volts positive with respect to its emitter; hence a point will be reached where CR20 becomes back biased. The base current to Q21 will then be limited to that value which can flow through R70. Similar limiters are associated with CR23, CR15, CR12, and CR7.

In order to ensure stability when a feedback loop is closed around any high-gain amplifier it is necessary that the frequency response and phase shift be carefully controlled. In the Model 630 this is accomplished with resistor-capacitor networks between stages. The capacitors associated with these rolloffs are C2, C7, C12, C14, C15, C16, C19, C22, C23, and C28.

3.3.3.3 Limiting and Integrating:

Since the recovery time of this type of amplifier is rather long when it is overloaded, it is desirable to prevent overloading. This is done by a limiting network associated with CR13, and CR14. These diodes are held back biased by voltages set by R80, R31, and R37, R38. The back bias is overcome on excessive negative and positive output swings, respectively, and current flows through the limit diodes to the summing junction. This current is sufficient to offset up to about 50 times the normal input current from the E_x source.

Since the VCO is designed to be responsive only to the integral of currents into the summing junction, the amplifier is operated as an integrator. This is accomplished by connecting a capacitor between the summing junction and the amplifier output. A simplified analysis of the operation can be made by assuming that the summing junction is ground, or zero volts (sometimes called virtual ground). This is a reasonable assumption since it is only necessary to move the summing junction a fraction of a microvolt to drive the output of the amplifier to its limit due to its high gain factor; thus, it can be seen that currents flowing through resistors such as R79 and R33 or R81 will be proportional to the voltage supplied by E_x, or by the electronic switch. Also, the voltage across C11, which must be the amplifier output voltage E_o, is $E_o = Q/C$, but the charge Q is defined to be $Q = \int i dt$, where the current i must come through R79 or R127. Hence, $E_o = 1/C \int i dt$. Since on a steady-state basis no net current can flow through C11 the current through R127 must be equal and opposite to the current flow through R79 in order for the sum of the currents into the summing junction to be zero (steady state). If these currents do not add to zero at any instant in time, then the current must flow into or out of C11, requiring the amplifier output voltage to change in order to keep the summing junction at zero. This change in voltage is applied to the VCO and corrects its frequency to bring the overall system back into balance.

3.3.4 Voltage Controlled Oscillator (VCO)

The VCO is a free-running multivibrator made up of transistors Q9 and Q10 on the integrator amplifier board. The operating frequency of the multivibrator is controlled by the DC voltage level at the collector of Q8, a combination amplifier-filter and inverter circuit. The voltage present at the collector of Q8, in turn, is determined by the output from the wide-band amplifier (TP3). The output voltage from Q8 is filtered by an RC network consisting of R99 and C25. Output from the VCO at the junction of R112 and CR32 is routed to the frequency board where it triggers a Schmitt circuit whose output pulses are the ones actually accumulated by the display counters during the sampling interval. These pulses are also divided down by a factor of 64 by a counter on the inside power supply board to control the duty cycle of the pulse width generator on board 104-126.

3.3.5 Pulse Width Generator

The pulse-width generator produces, after every sixty fourth VCO pulse, a square pulse having a precisely fixed time duration. The pulse width is fixed by counting a fixed number of pulses from a 1-megacycle crystal controlled oscillator during the on time of the duty-cycle flip-flop.

The output of the pulse width generator, the zero side of the pulse-width flip-flop Q10 and Q11 is AC coupled to the precision flip-flop Q12 and Q13, located on the integrator amplifier board. This flip-flop, in turn, drives the precision switch Q14, Q15.

The duty-cycle flip-flop is set by the signal out of the VCO divider. The zero side of this flip-flop then enables the 2^1 flip-flop in the pulse-width divider chain to be set by the next clock pulse. The 2^1 flip-flop then enables the input gate to the pulse-width flip-flop. The following clock pulse sets the pulse-width flip-flop to its 1 state, which supplies a negative-going pulse to the precision switch circuit on the integrator amplifier board and removes a clamp from the 2^0 flip-flop in the pulse-width divider chain. With the clamp removed the divider chain is allowed to count clock pulses until the stop position is reached. This occurs when all flip-flops in the divider chain are in their 1 state. The next clock pulse resets the pulse-width flip- flop. Resetting the pulse-width flip-flop supplies a positive pulse to the precision switch, clamps the 2^0 bit, resets divider chain bits 2^2 through 2^7, and conditions the pulse-width generator circuit so the sequence can be repeated on receipt of the next pulse out of the VCO divider.

3.3.6 Precision Switch and Reference Voltage Supply

The reference voltage for the precision electronic switch (Q14, Q15, on integrator amplifier board) comes from a separate winding on the power transformer. This voltage is applied to a zener diode, CR15, located in a bridge circuit (on board 104-125) which is designed to cancel out the effects of the finite Zener dynamic impedance. The output of this bridge circuit is the reference voltage E_r. Across this supply is connected a divider, the approximate center of which is ground. From this, voltages of $+E_r/2$ and $-E_r/2$ are developed with respect to ground. By referring to the integrator amplifier schematic it can be seen that when Q14 is non-conducting Q15 will conduct and current will flow from the summing junction through Q14 and R27. With Q14 conducting Q15 is cutoff and current flows in the opposite direction through R27 and Q15. If Q14 is switched on and off at approximately a 50% duty cycle the net current flowing through R27 will be zero. Increasing the ratio of on to off time of Q14 will drive the average voltage applied to R27 positive, and increasing the ratio of the off to on time causes the current to flow in the opposite direction, on the average. Thus, by the proper adjustment of the ratio of on to off time of Q14 it is possible to make the current through R27 equal and opposite to the current through R33 or R81, which will be proportional to the unknown voltage. It should be noted that the feedback signal through R27 can be either positive or negative, depending on the polarity of the unknown voltage E_x.

3.4 TIME BASE (DC VOLTAGE MODE)

The time base circuit is shown in figure 3.6. The time base (TB) flip-flop is controlled by an electronic counter consisting of two divide-by-10 circuits and a series of divide-by-2 circuits connected in cascade. The TB flip-flop supplies the output from the circuit and the primary function is to unclamp a gate, located electrically between the Schmitt trigger circuit and transformer T3, so that the pulses generated by the VCO during the sample period can transfer into the display counter.

The first divide-by-10 section of the counter divides 1 MC clock pulses down to a frequency of 100 KC. The second divide-by-10 section divides the 100 KC frequency down to 10 KC. The 10 KC pulses are then counted by the divide-by-2 flip-flops until the end of the sample period at which time the counter resets the TB flip-flop.

The circuit starts operating upon receipt of a sample command through transformer T4. This resets the 2^9 flip-flop in the time base counter chain, thereby enabling a gate at the input of the TB flip-flop and clamping the display multi in its off state. The next pulse produced at the output of the VCO divide-by-64 counter (at Q15, Q16) on the inside power supply board) sets the TB flip-flop. When the flip-flop sets, it (1) removes a clamp from the first flip-flop in the time base counter chain so the counter can start counting, (2) removes a clamp from the input of transformer T3 driver so the VCO pulses can transfer into the display counter, and (3) clamps the output of the display multi at pin 12 on the inside power supply board to prevent it from pulsing transformer T2.

At the end of the 0.1 second or 1 second sample period, as selected with the FUNCTION switch, the time base counter stops counting the clock pulses and resets the TB flip-flop. This occurs for the 0.1 second sample period when the first, fourth, eighth, twelfth, fourteenth, fifteenth, sixteenth, and seventeenth flip-flops in the counter chain are simultaneously in their set states. For a 1 second sample period the TB flip-flop is reset when the first, fourth, eighth, thirteenth, seventh, and eighteenth flip-flops are simultaneously in their set states.

When the TB flip-flop resets, it (1) places the 2^9 flip-flop in its set state and resets all other flip-flops in the time base counter, (2) returns the clamp to the first flip-flop in the counter chain to deactivate the counter, (3) reclamps the input to transformer T3 to prevent further VCO pulses from passing through to the display counter, and (4) removes the clamp from the output of the display multi so it can pulse transformer T2 to start the storage and display cycle.

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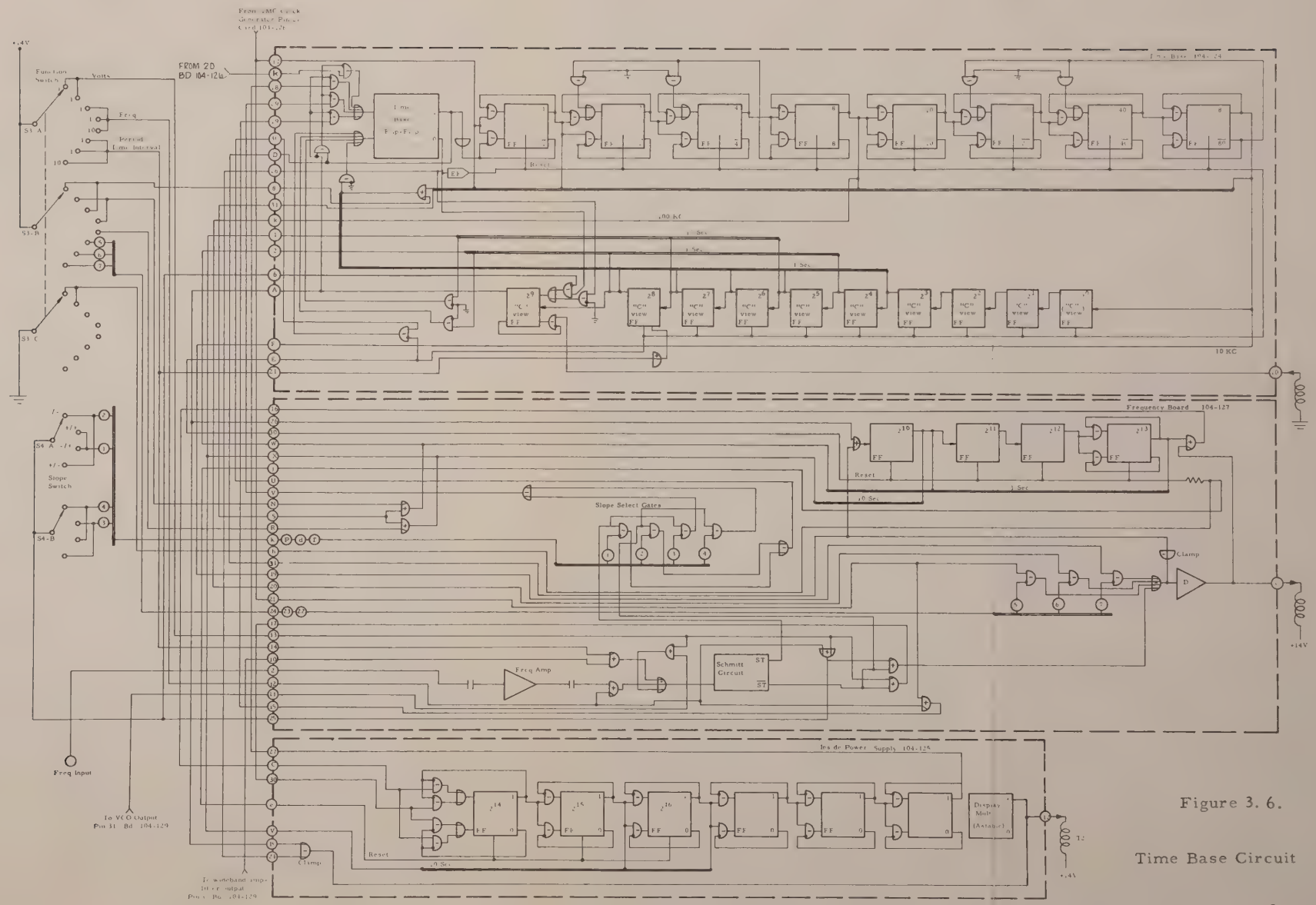


Figure 3. 6.

Time Base Circuit

3.5 SAMPLE LOGIC

The circuits on sample logic board 104-121 perform the following functions:

a. A sequencer generates a series of signals in a fixed time sequence to control the various operations required during the storage and display cycle. The sequencer also supplies a pulse at the end of each storage and display cycle to initiate the next sample period when the meter is in the continuous encoding mode.

b. A polarity and overrange flip-flop circuit determines the polarity of DC voltage measurements, whether the measurement is greater than full scale, and supplies corresponding signals to energize the polarity and overrange symbols in the readout.

c. An inverter circuit (Q1) conditions all pulses counted by the display counter before they are applied to the counter.

3.5.1 Sequencer

The sequencer is shown in figure 3.7. The circuit includes a lock flip-flop and four monostable multivibrators labeled on the illustration as clear mono, store mono, reset mono, and var mono. The cycle starts at the end of the sample period when a negative pulse is received at transformer T2 from the display multivibrator, located on the inside power supply board. The pulse passes through gates E and G where it resets the lock flip-flop (Q5, Q6 on sample logic schematic), and through gates I and J where it triggers the clear mono (Q16, Q17). The trailing edge of a negative pulse from the clear mono then passes through gate K and triggers the store mono (Q18, Q19) which, in turn, at the end of its pulse time, sends a positive-going pulse edge through gate M to trigger the reset mono (Q20, Q21). The trailing edge of a negative pulse generated by the reset mono then passes through gates C, D, and G and sets the lock flip-flop to return it to its orginal state. If the continuous encode mode is being used (ENCODE control set to CONT) a negative pulse from the lock flip-flop next transfers through transformer T4 to the time base circuit where it initiates the next sample period. The lock flip-flop when in its set state, enables gate I. This allows the clear mono to trigger on the next display multivibrator pulse at T2.

When the sequencer is operating in the variable encode mode (ENCODE switch set to VAR) the sample command pulse from the lock flip-flop does not go directly to T4 but passes through gate N and triggers the var mono. This circuit then supplies the sample command to T4. A variable RC network consisting of the resistance of the variable ENCODE control and a fixed capacitor determine the time duration of the var mono.

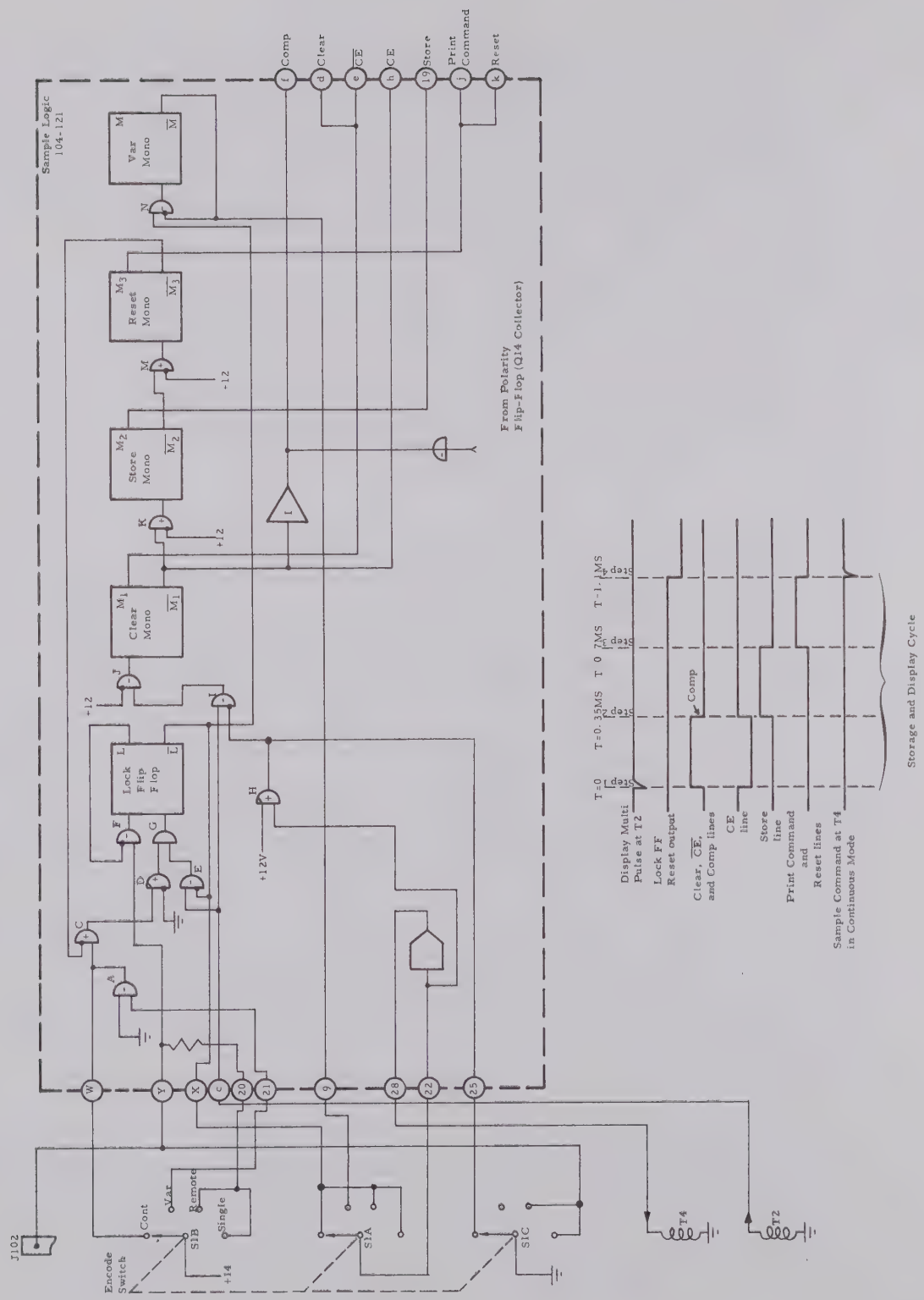


Figure 3.7. Sample Logic Sequencer

If the sequencer is operating in the remote or single encode mode (ENCODE switch set to REMOTE or rotated to SINGLE) the lock flip-flop is not returned to its set state by a pulse at the end of the cycle but, instead, by a negative-going signal or a contact closure to ground, applied either through the SINGLE position of the ENCODE switch or at pin z of connector J102. This sets the flip-flop through gate F.

As the sequencer proceeds through each of its steps either negative or positive pulses or both, are supplied to output lines in accordance with table 3.1 and the order shown in figure 3.7.

Table 3.1. Sequencer Truth Table

STEP	LOCK FF	CLEAR MONO	STORE MONO	RESET MONO
0	1	0	0	0
1	0	1	0	0
2	0	0	1	0
3	0	0	0	1
4	1	0	0	0

Note: 1 indicates that flip-flop is set or mono is in unstable state.

Note: 2 indicates that flip-flop is reset or mono is in stable state.

At step 1 the lock flip-flop resets and the clear mono is triggered to its unstable state. A positive signal then appears on the clear and $\overline{CE}$ lines, and if a negative DC voltage is being measured, on the comp line. At the same time, zero volts appear on the CE line. The signals on the CE and $\overline{CE}$ lines are routed to the display counter where they disable interconnecting AND gates between all decades and between the individual flip-flops making up the decades. The negative-going edge of the comp signal is used on negative DC polarity to generate the nines complement of the count existing in the display counter at the end of the sample period. For all other measuring modes the comp line is clamped to ground through a diode and transistor in the polarity flip-flop. The positive signal on the clear line at step 2 resets all storage driver flip-flops on the display counter boards (see figure 3.9). As the clear mono returns to its quiescent state at step 2, it triggers the store mono. A positive signal then appears on the store line. This enables the decoder gates at the input of

the storage register so the measurement information existing in the BCD counter can be converted to decimal and transfer into the storage register. Transistor drivers associated with the storage register are used to energize the Nixie lamps in the front panel readout.

At step 3 the store mono returns to its quiescent state and triggers the reset mono. A positive signal then appears on the print command and reset lines. This signal (ground to + 12 volts) is routed to pin k of output connector J102 on the rear panel and to the polarity-overrange circuit where it resets the polarity and error flip-flops. It is also routed to the display counter where it resets the BCD counter to either its 00000 or 80000 state, depending on the measuring mode being used. For the DC voltage mode using a 0.1 second sample period the pulse sets the counter to 80000. For all other modes the counter is set to 00000.

3.5.2 Polarity and Overrange Display

Polarity and overrange in the Model 630 are display functions for DC voltage measurements only, and are controlled by the error and polarity flip-flops (Q7, Q8 and Q14, Q15 on sample logic schematic). These flip-flops operate together as a 2-stage binary counter. The circuit, shown in figure 3.8 is designed to count carry-over pulses supplied by either the 10^3 decade or 10^4 decade of the display counter, depending upon which sample period is being used for the measurement. If a 0.1 second sample period is being used, a pulse is supplied by the 10^3 decade each time it counts through 9 back to 0. The pulses are supplied in a similar manner by the 10^4 decade when a 1-second time base is being used. The output signals from the polarity and error flip-flops control two storage driver flip-flop circuits (Q9, Q10, and Q11, Q12 on sample logic schematic). These, in turn, supply the energizing signals to the error (E) and polarity (+), (-) lamps on the front panel.

At the start of the sample period the error flip-flop is placed in its set state and the polarity flip-flop in its reset state by a positive signal on the reset line from the sequencer (refer to paragraph 3.5.1). During the sample period the counter can be switched to four possible states. This is shown in table 3.2.

The initial state of the counter corresponds to a negative polarity overrange voltage measurement. For the negative overrange condition the display counter supplies no carry-over pulses since a maximum of 9999 pulses are generated by the VCO during a 0.1 second sample period and a maximum of 99999 pulses during a 1 second sample period. As explained in paragraph 3.6 the display counter starts counting from a preset count of 80000 at the beginning of 0.1 second sample period. Adding the maximum 9999 VCO pulse count possible during this period would still not cause the 10^3 display counter decade to reset back to 0.

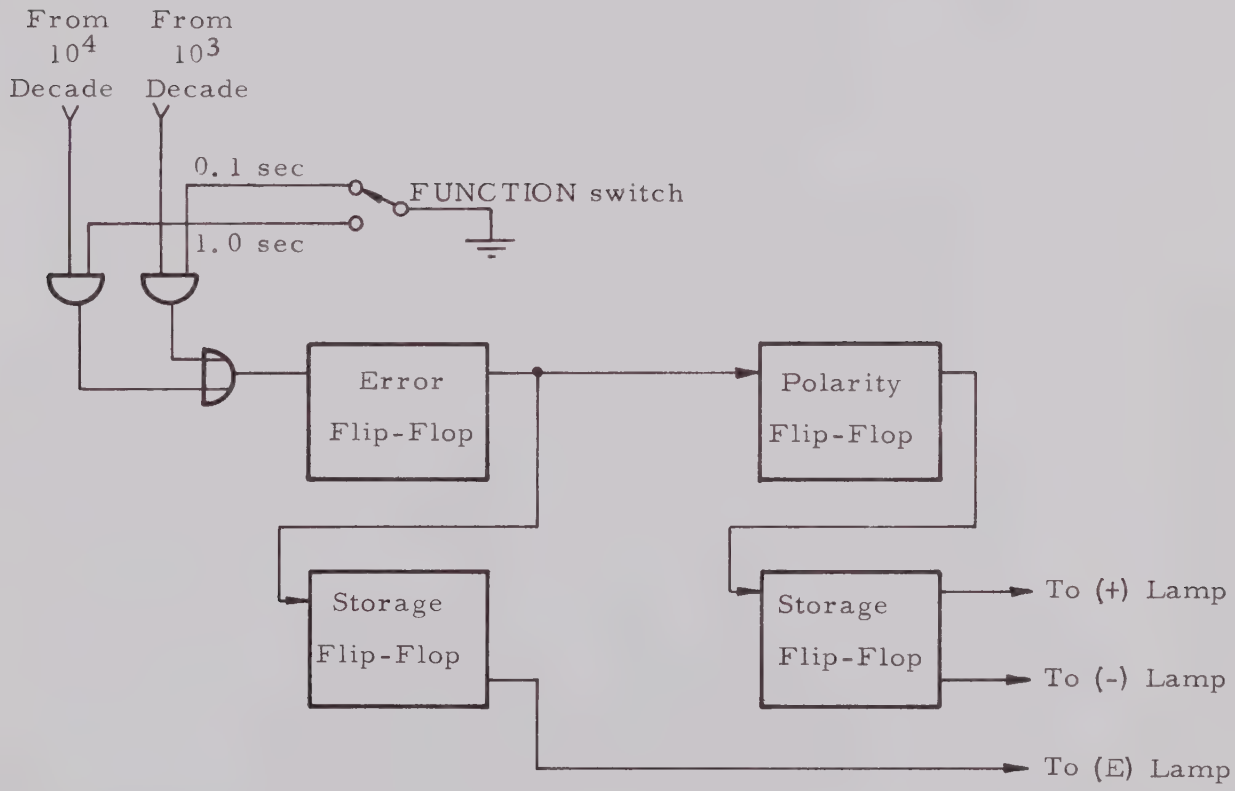


Figure 3.8. Polarity and Error Network

Table 3.2. Truth Table for Polarity and Overrange Flip-Flop Counter

Carry-Over Pulses from 10^3 or 10^4 Decade	Error Flip-Flop	Polarity Flip-Flop	Display Produced
0	1	0	Negative Overrange
1	0	0	Negative In-range
2	0	1	Positive In-range
3 or more	1	1	Positive Overrange

For negative voltage measurements under full scale the number of VCO pulses that will be counted by the display counter will fall somewhere between 10000 and 19999 if a 0.1 second sample period is being used, and between 100000 and 199999 for a 1 second sample period. Adding the preset count of 80000 to the VCO pulse count accumulated during the 0.1 second sample period shows that the final count in this case will be some number greater than 90000 but not over 99999. For a 1 second sample period, it will be greater than 100000 but not over 199999. Both of these limits indicate that the 10^3 decade during the 0.1 second sample period, or the 10^4 decade during the 1 second sample period, will have reset from 9 back to 0 one time and one carry-over pulse will have been sent to the polarity and overrange counter. This resets the error flip-flop and switches the counter to the negative in-range state, as table 3.2 indicates.

For positive voltage measurements less than full scale, when using a 0.1 second sample period, from 20000 to 29999 VCO pulses will be counted over a 0.1 sample period, and from 200000 to 299999 pulses during a 1-second sample period. Adding the 0.1 second sample period pulse count to the preset 80000 makes the total accumulated count fall somewhere between 100000 and 109999. During a 1-second sample period, the total accumulated count will be the actual number of VCO pulses counted. The 10^3 or 10^4 decade, depending upon which time base is being used, will therefore count through 9 to 0 two times and thus, two carry-over pulses will be supplied to the error and polarity flip-flops, causing the error flip-flop to reset and the polarity flip-flop to set. Table 3.2 shows this to be the positive in-range voltage state.

For positive voltage measurements in excess of full scale 30000 or more VCO pulses will be counted during a 0.1 second sample period and 300000 or more during a 1-second sample period. Adding the pulses

counted during the 0.1 second period to the preset 80000 results in a total accumulated count of 110000, or greater. From this, it can be seen that while the count in the display counter has increased from 80000 to 110000 the 10^3 decade has counted through 9 to 0 three times and three carry-over pulses have been produced to advance the error and polarity counter to its positive voltage overrange state. The 300000 or more VCO pulses which are counted during a 1 second sample period would have the same effect by causing the 10^4 decade to count through 9 to 0 three times.

Table 3.2 shows the error flip-flop in its 1 state for an overrange measurement. In this state it enables a gate at the input of storage driver flip-flop Q11, Q12, allowing that flip-flop to be set by the next pulse on the store line from the sequencer. When the storage driver flip-flop is set, it provides a ground return through a transistor for one side of the ERROR display lamp. This produces a 70-volt step change at the cathode of the lamp and results in an igniting potential of 120 volts being applied across the lamp terminals. The flip-flop remains in this state and keeps the ERROR lamp illuminated until some time during the next storage and display cycle, at which time it is reset by a pulse on the clear line from the sequencer.

The two POLARITY display lamps are driven by one side or the other of storage driver flip-flop Q9, Q10 to ensure that only one lamp will be energized at a given time. This flip-flop is controlled by the polarity flip-flop. Depending upon the polarity of the measured voltage, the polarity flip-flop will be either set or reset and enable a corresponding gate at the input of the storage flip-flop. The next pulse from the sequencer on the store line is then allowed to pass through the enabled gate and set or reset the storage flip-flop. Conduction through one of the two transistors in the flip-flop then serves as a ground return for the cathode of the selected POLARITY lamp. This energizes the lamp in the same manner as described for the ERROR lamp in the preceding paragraph.

The + or - symbol is normally suppressed when the "E" (full scale exceeded) symbol appears since, in system operation, this symbol is normally printed in the same column as + or -. If it is not desired that the + or - be suppressed, remove diodes CR17 and CR20 on the sample logic board.

3.6 DISPLAY COUNTER AND STORAGE

The display counter and storage network are shown in figure 3.9. The counter consists of five decades of BCD counters with associated decimal storage flip-flops. The decades are connected in cascade to produce the five digits making up the displayed measurement. Each decade comprises four flip-flops interconnected by gating circuits to form a modulo-10 counter which counts from 0 through 9 in 2*421 binary code (see table 3.3).

Table 3.3. 2*421 Truth Table

NUMBER	2*	4	2	1
0	0	0	0	0
1	0	0	0	1
2	1	0	0	0
3	1	0	0	1
4	1	0	1	0
5	1	0	1	1
6	1	1	0	0
7	1	1	0	1
8	1	1	1	0
9	1	1	1	1

Note: 1 indicates flip-flop is in set state. 0 indicates flip-flop is in reset state.

Outputs from the BCD counter flip-flops are routed at the end of the counting cycle through a matrix BCD to decimal decoder. When the state of the counter is examined by the decoder, ten discrete signal combinations representing the numbers 0 through 9 are produced by each decade. Upon receipt of a positive voltage level on the store line from the store mono in the sequencer, these signal combinations activate the front panel display by driving corresponding transistorized Nixie driver storage circuits into conduction.

To provide for automatic polarity determination (see paragraph 3.5.2) the BCD counter starts counting from a preset 80000 when the 0.1 second sample period is being used (FUNCTION switch set to VOLT 0.1 SEC SAMPLE). For all other measuring modes the counter starts counting from a preset 00000. This is done at the beginning of the sample period

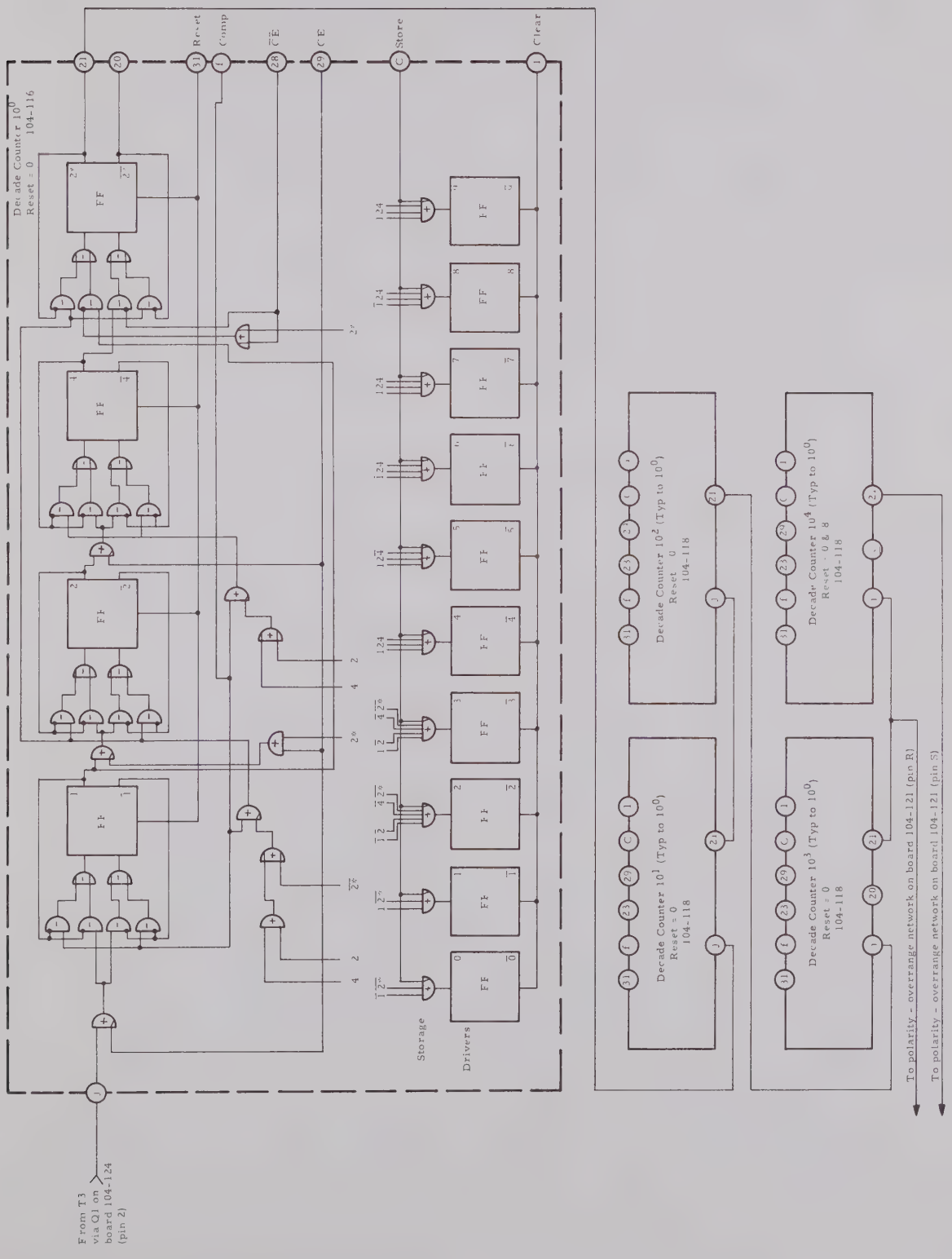


Figure 3.9. Display Counter

by a signal on the reset line from the sequencer. To preset the counter to 80000 the signal sets the 2*, 4, and 2 flip-flops in the 10^4 decade and resets all other flip-flops in the counter. The signal resets all flip-flops in all decades when presetting the counter to 00000.

During DC voltage measurements the 10^0 decade counts the pulses from the Schmitt trigger (on frequency board) which is driven by the VCO during the sample period. When frequency is being measured, this decade counts the waveforms of the signal applied to the FREQ input terminal after they have been converted to rectangular pulses by a limiting amplifier and the above mentioned Schmitt circuit. During period and time interval measurements the 10^0 decade counts either 10 KC, 100 KC, or 1 MC pulses which are generated by the time base counter on board 104-124. The frequency which will be counted depends on the time base selected with the front panel FUNCTION switch. 10 KC pulses will be counted for a 10 second time base, 100 KC pulses for a 1 second time base, and 1 MC pulses for a 0.1 second time base.

For every 10 pulses counted by the 10^0 decade, one carry-over pulse is generated. This is counted by the 10^1 decade. In like manner, the 10^2 decade counts the carry-over pulses from the 10^1 decade, the 10^3 decade counts the 10^2 decade carry-over pulses, and the 10^4 decade counts the 10^3 decade carry-over pulses. The carry-over pulses produced by the 10^3 and 10^4 decades are also routed to the sample logic board during voltage measurements for polarity and overrange determination (refer to paragraph 3.5.2).

At the end of each sample period the interconnecting gates between the BCD counter decades and between each pair of flip-flops in the decades are disabled by negative and positive voltage levels from the sequencer on the CE and $\overline{CE}$ lines, respectively. This is done to ensure that the accumulated information in the counter will not be disturbed by transients during its transfer to the storage and display circuits. If the measured signal is a negative DC voltage, the polarity and overrange sensing circuit next removes a clamp from the output of an inverter in the comp line at the sample logic sequencer. The negative-going trailing edge of the first pulse generated by the sequencer on this line switches the BCD counter flip-flops to a state representing the nines complement of the count existing in the counter at the end of the sample period. The reason for doing this is that the frequency of the VCO which was counted during the sample period varies inversely with DC voltage of negative polarity. The complemented count is the true value of the negative voltage. The nines complement binary code is listed in table 3.4. On other than negative voltage measurements the complement line is clamped to ground by the polarity flip-flop in the polarity and overrange circuit and the counter retains the accumulated count.

Table 3.4. Nines Complement Truth Table

NUMBER	2*	4	2	1
0	1	1	1	1
1	1	1	1	0
2	1	1	0	1
3	1	1	0	0
4	1	0	1	1
5	1	0	1	0
6	1	0	0	1
7	1	0	0	0
8	0	0	0	1
9	0	0	0	0

Note: 1 indicates flip-flop is in its set state.

0 indicates flip-flop is in its reset state.

Before the complement command, at the trailing edge of the clear command, the next pulse from the sequencer on the clear line sets the storage register flip-flops on all display counter boards to remove the information still held in storage and being displayed from the previous encoding. Setting these flip-flops stops conduction in the transistors which are driving the cathodes of the energized Nixie indicators.

A positive pulse from the sequencer on the store line next enables the decoder matrix gates at the outputs of the display counter decades. This allows the information in the counters to pass through and reset the flip-flops in the storage registers in accordance with the numbers decoded by the gates. Transistors associated with those flip-flops having true input gates are then driven into conduction to energize the appropriate numeral in the readout. All flip-flops remain in their set or reset states until a pulse is received from the sequencer on the clear line during the next storage and display cycle.

The storage and display cycle ends when the sequencer supplies a pulse on the reset line. This resets the display counter to either 00000 or 80000, as described above.

3.7 FREQUENCY MODE

Figure 3.10 shows the block diagram of the Model 630 in the frequency measuring mode. The incoming frequency F_x is first passed through a limiting amplifier and a Schmitt trigger circuit to produce a squared waveform of useable amplitude. Output from the Schmitt circuit is then routed through an AND gate to the display counter (refer to paragraph 3.6). The gate is held open by the time base flip-flop for the duration of the sampling period which may be set to 0.1, 1, or 10 seconds with the FUNCTION switch. The number of pulses passing through the gate during the selected interval is a measure of the frequency of the input signal. The gate times are arranged so that the readout displays the measurement directly in kilocycles per second. The time base flip-flop is controlled by the time base counter (as described in paragraph 3.4 and 3.7.1.

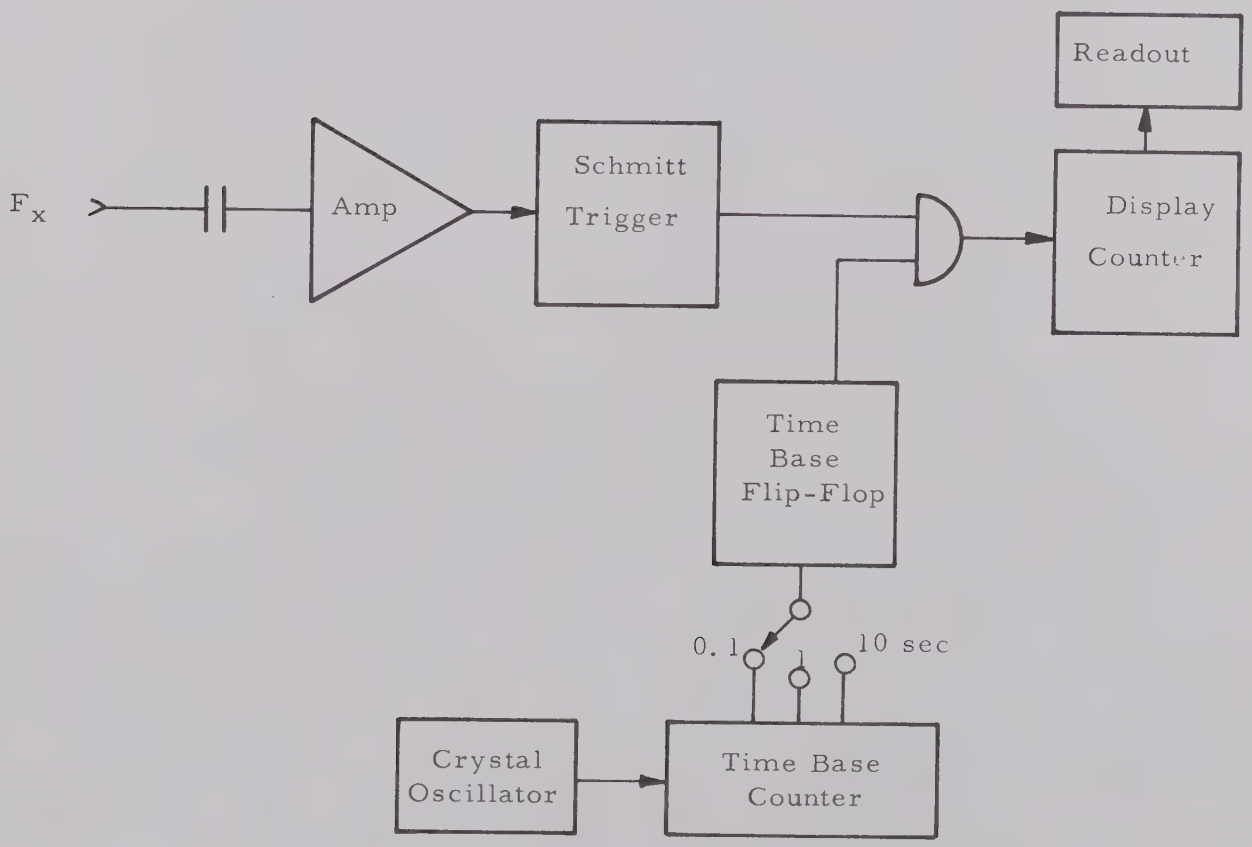


Figure 3.10. Model 630 in Frequency Mode

3.7.1 Time Base (Frequency Mode)

The time base circuit used for frequency measurements is basically the same circuit used for DC voltage measurements and described in paragraph 3.4. The circuit is shown in figure 3.6. In the frequency mode the time base controls the length of the sample period during which the unknown frequency is counted by the display counter. Three additional divide-by-2 stages (2^{14} through 2^{16}) are incorporated to provide 0.1 second, 1 second, and 10 second time base periods.

The circuit starts operating when a sample command pulse is received from the lock flip-flop (Q5, Q6) on sample logic board via transformer T4. This resets the 2^9 flip-flop in the time base counter chain, thereby enabling a gate at the input of the time base flip-flop and placing a clamp on the output of the display multi. The next 1 megacycle clock pulse generated by crystal oscillator Q5 on the pulse generator board sets the flip-flop.

When the time base flip-flop sets, it (1) releases a clamp on the first flip-flop in the counter chain, (2) removes a clamp from a gate located between the output of the Schmitt circuit and the input of the driver for transformer T3, and (3) places a clamp on the output of the display multi which drives transformer T2.

The time base counter then starts counting the 1 MC pulses from the crystal oscillator and the unknown frequency F_x starts pulsing the Schmitt circuit via the frequency amplifier. The pulses generated by the Schmitt circuit pass through transformer T3 to the display counter.

After either 0.1 second, 1 second, or 10 seconds, as determined by the setting of the front panel FUNCTION switch, a gate at the reset input of the time base flip-flop is pulsed by the counter. This resets the flip-flop to end the sample period. The reset signal is generated by the counter in the same manner as that described in paragraph 3.4. For a 10-second sample period, the time base flip-flop resets when the 1st, 4th, 8th, 14th, 16th, 18th, 19th, 24th, and 25th flip-flops are in their set states simultaneously and a clock pulse is applied.

In returning to its reset state the time base flip-flop (1) returns the 2^9 flip-flop to its set state (2) resets all flip-flops in the time base counter except the 2^9 flip-flop, (3) clamps the gate at the input of the transformer T3 driver, and (4) removes the clamp previously placed on the output of the display multi.

Following this, the next signal generated by the display multi pulses transformer T2. This resets the lock flip-flop on the sample logic board (paragraph 3.5) to start the storage and display cycle.

3.7.2 Frequency Amplifier

A simplified schematic of the frequency amplifier is shown in figure 3.11. The circuit is a 3-stage DC coupled amplifier with DC feedback and AC coupling capacitors at both the input and output. Refer to figure 3.6. The unknown frequency is applied from the rear panel frequency input connector through DC blocking capacitor C_a and series resistor R_a to the base of Q_a, the first stage of the amplifier. The feedback network R_c and R_b stabilizes the amplifier for DC temperature drift and is proportioned to hold the output of the amplifier at zero volts AC when a zero volt AC level is applied to the input. For frequencies in excess of approximately 10 CPS the reactance of capacitor C_d becomes negligible and effectively shorts the feedback signal to ground. The amplifier then has an open loop gain of 20. For input AC signals in excess of 100 millivolts RMS transistor Q_a saturates on the positive peaks to provide limiting action. On the negative peaks Q_a is cutoff and drives Q_b, the second stage in the amplifier, into saturation to provide the limiting action. This causes the amplifier output to have a rectangular waveform of approximately 6 volts peak-to-peak for input signals within the specified range of 300 millivolts P-P to 50 volts P-P. Capacitors C_b and C_c across input resistor R_a with diodes CR_a and CR_b protect the base of Q_a from high frequency transients which adversely affect the recovery time of the amplifier. The filter starts operating for transients having peaks in excess of 0.6 volt, with C_b or C_c in series with CR_a bypassing the positive peaks and C_b or C_c in series with CR_b bypassing the negative peaks.

The output of the amplifier is AC coupled to the Schmitt trigger circuit through a 1-stage pulse amplifier and an AND gate which is enabled when the FUNCTION switch is set to one of its frequency time base positions. The Schmitt circuit shapes the signal into a positive rectangular waveform (ground to +12 volts) with very fast rise and fall times.

3.8 PERIOD/TIME INTERVAL MODE

Figure 3.12 shows the Model 630 in its period/time interval measuring mode. The waveform being measured is fed to the integrating amplifier with feedback capacitor and pulse generator disconnected. Overloading of the amplifier is prevented by the limiting diodes. The selected slopes of the amplified waveform, as determined by the setting of the

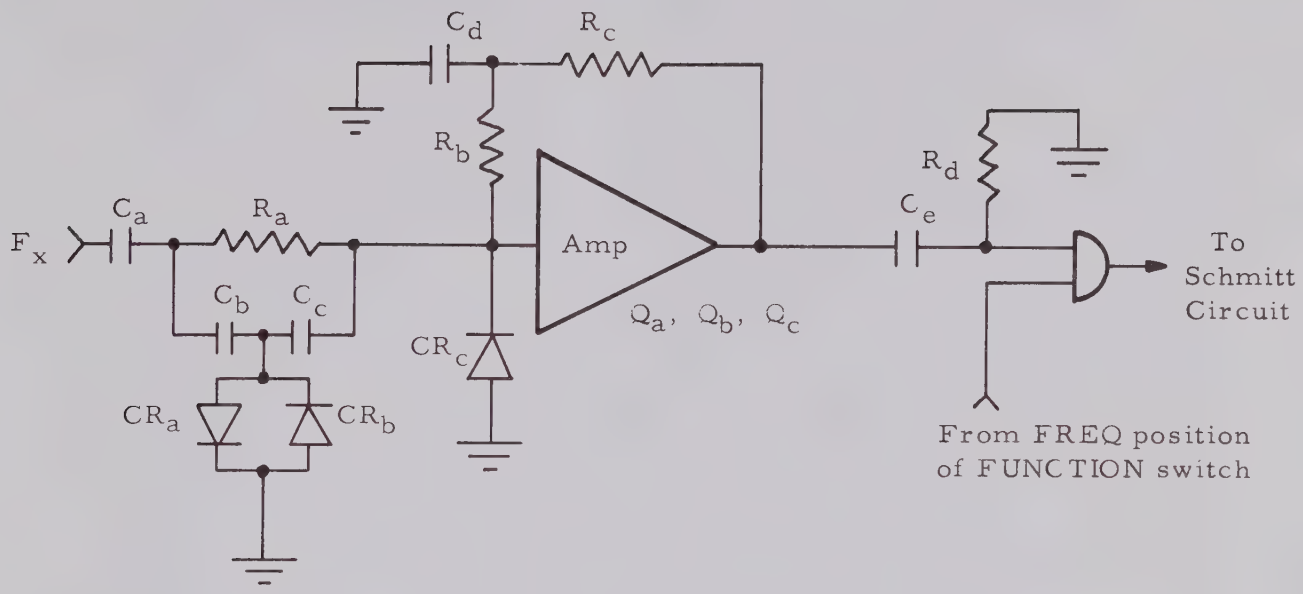


Figure 3.11. Limiting Amplifier Used in Frequency Mode

front panel SLOPE switch, triggers a Schmitt circuit whose output sets the time base flip-flop to start the measurement and resets the flip-flop to end the measurement. The AND gate is held open by this flip-flop for a time corresponding to the interval between the selected slopes of the input waveform and allows pulses from the time base counter (refer to paragraph 3.8.1) to pass through to the display counter (paragraph 3.6). The time base counter counts down the signal from a 1 MC crystal oscillator and generates output frequencies of either 10 KC, 100 KC, or 1 MC, corresponding to front panel FUNCTION switch time base settings of 10 seconds, 1 second, and 0.1 second, respectively. These frequencies are such that the readout will display the period or time interval directly in milliseconds.

3.8.1 Time Base (Period/Time Interval Mode)

Figure 3.12 shows the time base circuit used in the period/time interval mode. Also refer to figure 3.6 and paragraph 3.4. In this mode the time base flip-flop enables and inhibits various circuits throughout the meter and the time base counter operates as a frequency divider and supplies either 10 KC, 100 KC, or 1 MC pulses. These frequencies correspond, respectively, to the 10, 1, and 0.1 second full-scale settings

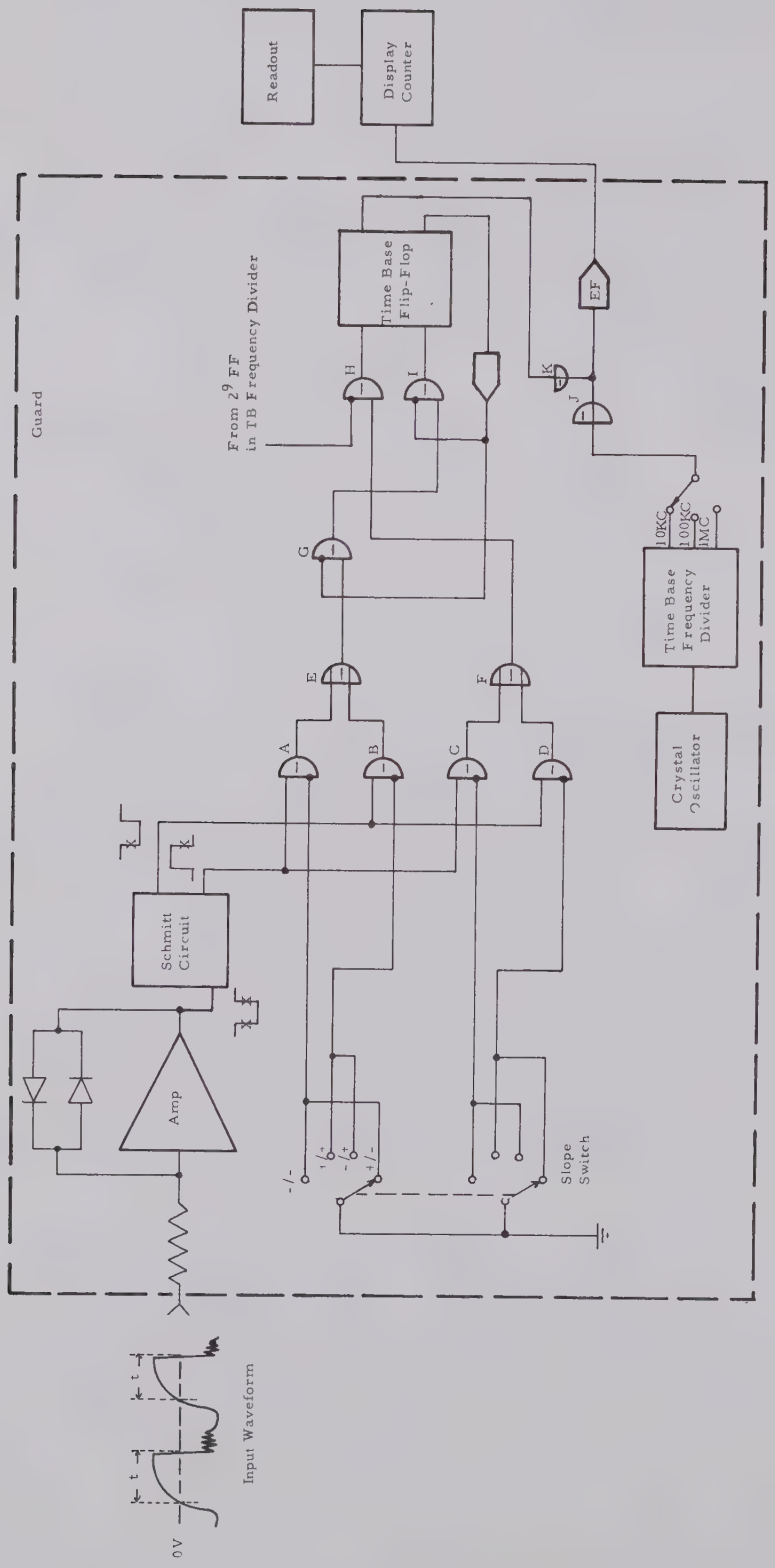


Figure 3.12. Model 630 in Period/Time Interval Mode

of the front panel FUNCTION switch. The number of these pulses counted by the display counter during the sample period is the measure of the elapsed time between the selected slopes of the input waveform.

The frequency pulses are generated by the frequency divider when the time base flip-flop is in its set state. The first four flip-flops in the divider are interconnected by gating circuits in a manner which permits it to divide 1 MC clock pulses down to 100 KC. The next four flip-flops operate similarly to the first four and divide the 100 KC pulses down to 10 KC. The 2^9 flip-flop in the divider chain is used to enable gates at the input to the time base flip-flop. It does this when it is reset by a sample command pulse via transformer T4 from the sample logic section, as described in paragraph 3.5.1. The time base flip-flop controls both the starting and stopping of the frequency dividing action, and, in turn, is controlled by the slopes of the waveform under measurement, as determined by the setting of the front panel SLOPE switch. To control the time base flip-flop, this waveform, after passing through a limiting amplifier, triggers a Schmitt circuit. The Schmitt circuit squares the waveform and presents it at output terminals in both an inverted and non-inverted form.

The leading and trailing edges of these pulses set and later reset the time base flip-flop by passing in ordered sequence through AND gates selected by the SLOPE switch. For example, assume that the pulse time of the waveform shown at the input of the Schmitt circuit in figure 3.12 is being measured. The SLOPE switch would be set +/- to enable AND gates A and D. The leading edge of the negative pulse at the output of the Schmitt circuit passes through gates D, F, and H. This sets the time base flip-flop and starts the frequency divider counting. At the end of the pulse time the trailing edge of the positive pulse produced by the Schmitt circuit is allowed to pass through gates A, E, G, and I. This resets the time base flip-flop and stops the divider action.

3.8.2 Limiting Amplifier

This amplifier is the same 2-channel chopper stabilized DC amplifier described in paragraph 3.3.3. In the period/time interval mode the amplifier is modified so it will function as an operational amplifier having a high gain factor for low level input signals and a low gain factor for high level input signals. The modification consists, basically, of disconnecting the integrating capacitor C11 by back biasing diode CR30, and disabling the precision electronic switch Q12, Q13, Q14, and Q15 by grounding the junction of R28 and R79 through diode CR24. The amplifier is prevented from overloading by the same diode-resistor network used in the DC voltage mode.

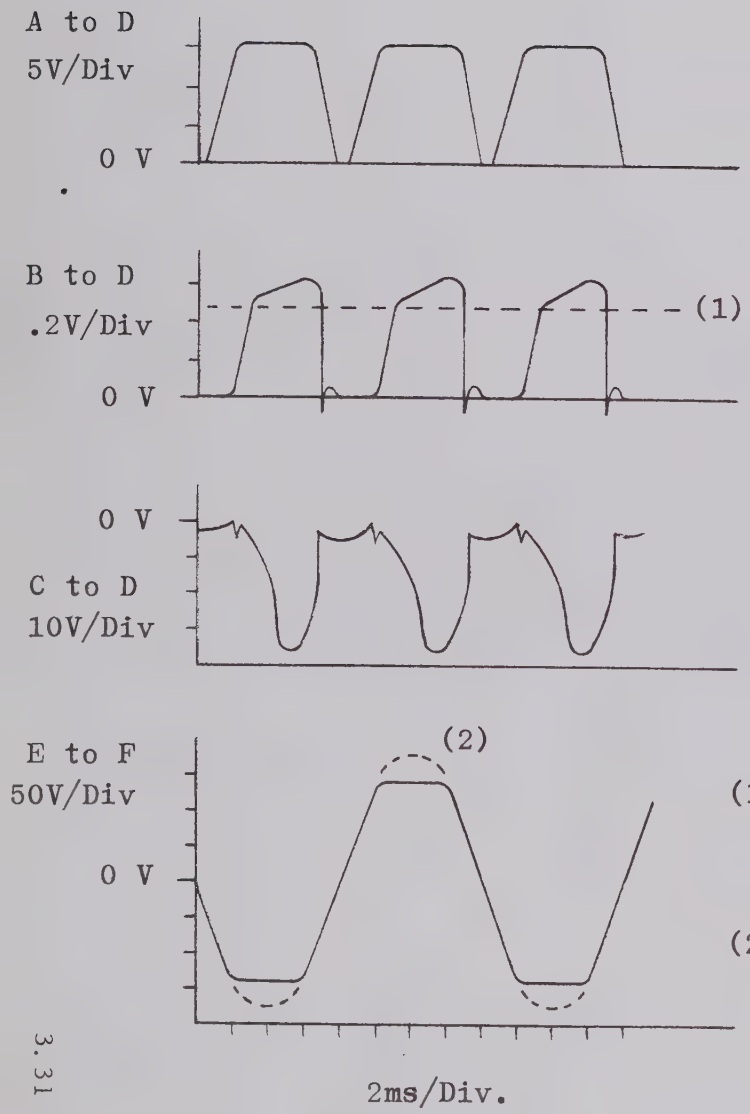
The circuit has high overall gain until diodes CR13 and CR27 or CR14 and CR26 conduct; thereafter, the gain is about 0.25. For a zero-volt input, the junction of R31, R37 is held essentially at ground level by the amplifier output. This causes diodes CR13 and CR14 to be back biased and introduces a high resistance into the feedback network, thereby eliminating the feedback voltage. When the input signal increases in amplitude, the output waveform increases until a point is reached where the output level forward biases CR13 on negative swings and CR14 on positive swings. The resistance inserted into the feedback network by the diodes then becomes small. This causes a drop in the amplifier gain factor to 0.25 and tends to flatten the top portion of the output waveform.

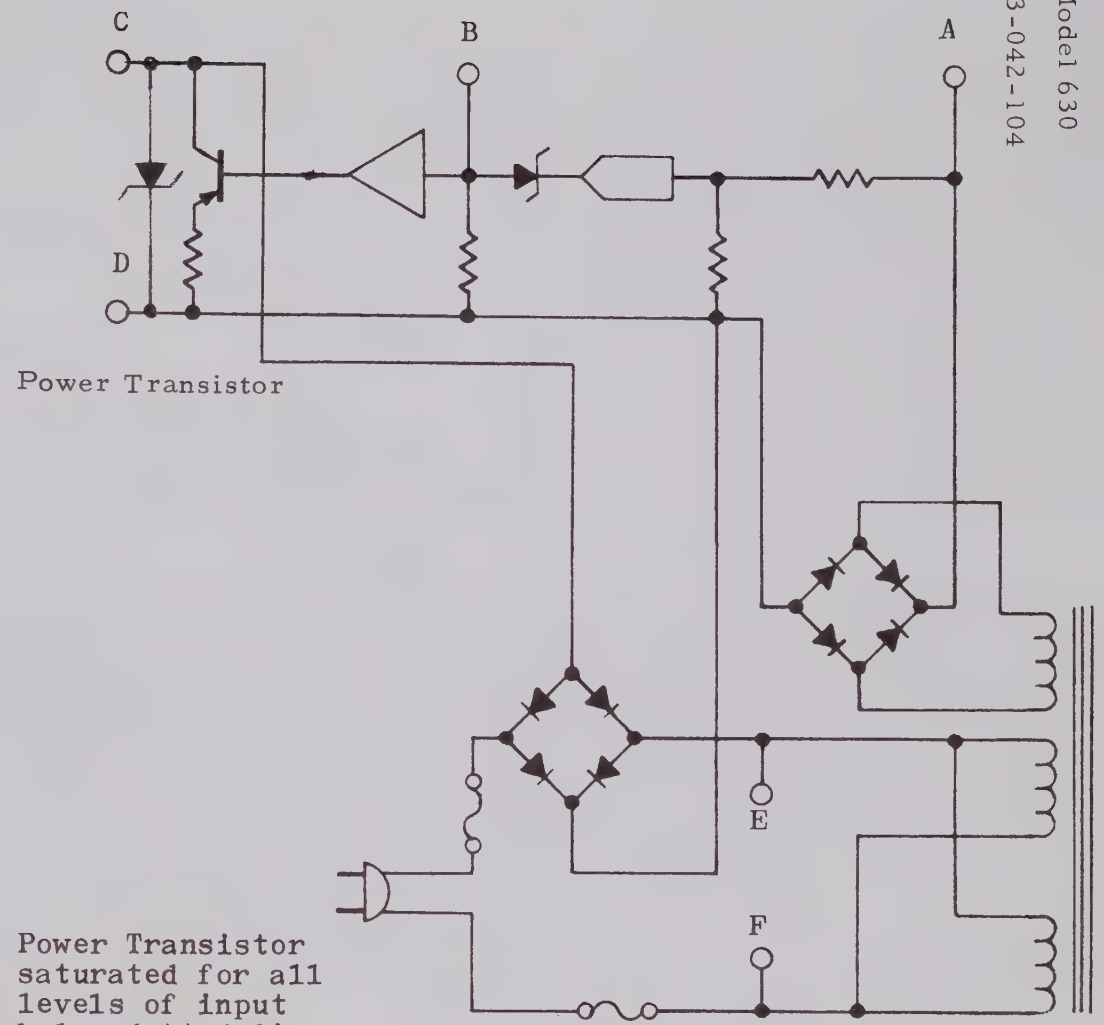
3.9 POWER SUPPLY

The DC supply voltages used in the Model 630 are derived from a single power transformer. The AC voltage at the transformer primary is regulated by using the voltage across a pilot winding on the transformer to control conduction through a transistor in series with the AC line (see figure 3.13). When wired for 117 volts AC operation the transformer will produce the required secondary voltages with a fixed primary voltage of 260 volts, peak to peak.

The series regulator (adjacent to transformer) is controlled by full-wave rectifying the AC signal from the pilot winding, and using the positive peaks of this pulsating DC signal to drive a series of five transistors on power supply and AC regulator board 104-104 (Q1 through Q6) which form a non-inverting voltage amplifier. Transistor circuit Q6, an emitter follower, is designed to minimize the current drain taken by the amplifier network from voltage divider R22, R18, R19, and R24. The zener, CR19, allows only that part of the signal exceeding 10 volts at the output of the emitter follower to pass through the amplifier chain. The last stage of the amplifier (Q1 and Q2) drives the base of the regulator transistor. Waveforms for the regulator circuit are shown in figure 3.13.

The regulator transistor 2N1159, operates in series with the line and the transformer primary through a diode bridge rectifier circuit consisting of diodes CR1 through CR4. The bridge is arranged so that all line current must flow in the correct direction through the transistor. Conduction through the transistor is automatically adjusted with line voltage changes and the voltage drop across the transistor is subtracted from the line voltage to compensate for the change.





(1) Power Transistor saturated for all levels of input below dotted line.

(2) Dotted line indicates unclipped line waveform.

Figure 3.13. AC Regulator

Paralleled capacitors, C6 and C7, are charged through diode CR20 to the peak positive value of the pulsating DC signal, approximately 18 volts. This voltage serves as the DC supply for the regulator amplifier circuits.

The AC voltages at the secondary windings of the transformer are converted to DC voltages by conventional bridge rectifiers and filter networks located on both the inside power supply board (104-125) and the power supply and AC regulator board (104-104). The inside power supply board furnishes the voltages for those circuits inside the guard, and the power supply and AC regulator board furnishes the voltages for those circuits outside the guard.

Voltages produced by the inside power supply board are listed in table 3.5 and those produced by the power supply and AC regulator are listed in table 3.6.

Table 3.5. Voltages Supplied by Inside Power Supply Board 104-125

VOLTAGE	TEST POINTS
+14 Volts	Pin 29
-14 Volts	Pin 28
+45 Volts	Pin 26
+4.3 Volts (Approx. Refer. Voltage)	Pin 17
-4.3 Volts (Approx. Refer. Voltage)	Pin 10
Ground	Pins D through T

Table 3.6. Voltages Supplied by Outside Power Supply and AC Regulator Board 104-104

VOLTAGE	TEST POINT
+12 Volts	Pin 28
-12 Volts	Pin 18
+90 Volts	Pin 25
+250 Volts	Pin 30
+70 Volts	Pin 22
Ground	Pins D through c

SECTION IV

CALIBRATION

4.1 GENERAL

Proper operation of this instrument depends on accurate calibration being maintained. Adjustments are required if one or more of the following conditions exist, and provided the trouble is not caused by a defective component:

a. The meter does not display a reading of 00000, to within the limits stated in the specification, on any DC voltage range with the GUARD, HI, and LO input terminals shorted together. This indicates that one of the ZERO offset controls is out of adjustment.

b. The meter does not measure within specifications on one or more DC voltage ranges. This indicates that either the 100MV, 1000MV, 10V, 100V, or 750V calibration control is out of adjustment.

c. A defective 1N 938 Zener has been replaced in the reference bridge circuit on inside power supply board 104-125.

d. One or more precision resistors has been replaced.

NOTE

The Zener should be replaced only with a similar Zener which has been pre-tested and supplied by Electro Instruments, Inc. The current through the Zener is adjusted with the reference Zener current control, located on the inside of the meter adjacent to the right side panel (43, figure 4.1). The required current for the replacement Zener will be specified by the factory.

WARNING

With signal leads connected to the meter any common mode voltage existing between the signal source and ground will also be present between the guard housing, inside

circuitry, and earth ground. This presents no hazard as long as the front service door is closed and the guard shield is kept well insulated, since the guard housing and inside circuitry cannot be reached when the door is closed. Before the front door is opened the servicing personnel should either disconnect the signal leads from the meter, or confirm that no hazardous common-mode voltages exist at the signal sources.

4.1.1 Equipment Required:

a. Milliammeter, 0 to 10 milliamperes, 3% accuracy, or better. (If Zener 1N938 is replaced).

b. Precision DC voltage standard, continuously variable from 0 to 750 volts, and having an output impedance not exceeding 1 ohm on ranges up to 0.1 volt full scale, 10 ohms on the 1 volt full scale range and 100 ohms on ranges greater than 10 volts. The standard should have resolutions corresponding to the following:

1 μvolt between 0 and 100 millivolts

10 μvolts between 100 millivolts and 1 volt

100 μ volts between 1 volt and 10 volts

1 millivolt between 10 volts and 100 volts

10 millivolts between 100 volts and 750 volts

4.1.2 Zero Offset Adjustment

a. Connect instrument to appropriate AC power source and set POWER switch to ON. Allow at least 15 minutes for warmup.

b. Set RANGE switch to 1000MV position

c. Set FUNCTION switch to 1 SEC VOLT position

d. Set ENCODE switch to CONT.

e. Short together the HI, LO, and GUARD input terminals, located on the rear panel.

f. Unlatch the service door by pressing the button at the left side of the front panel. Swing the door outward on hinge to gain access to the 10 volt range ZERO offset control (42, figure 4. 1), which is located on the back side of the front panel.

g. Observe front panel display and rotate the ZERO control until a reading of 0. 0000 is obtained and the polarity symbol shifts back and forth between + and - at a constant rate.

h. Set RANGE switch to 100 MV.

i. Observe front panel display and adjust the 100 millivolt range zero offset control (46, figure 4. 1) until a reading of 00. 000 ± 3 digits is obtained and the polarity symbol shifts back and forth between + and - at a constant rate.

4. 1. 3 Range Calibration

NOTE

Do not make the following adjustments until the ZERO offset adjustment procedures in paragraph 4. 1. 2 have been completed.

a. Set RANGE switch to 100MV.

b. Set FUNCTION switch to 1 SEC VOLT.

c. Set ENCODE switch to CONT.

d. Connect DC voltage standard to HI, LO, and GUARD input terminals on rear panel (positive to HI, signal ground to LO, shield to GUARD). Connect jumper between GUARD and LO terminals.

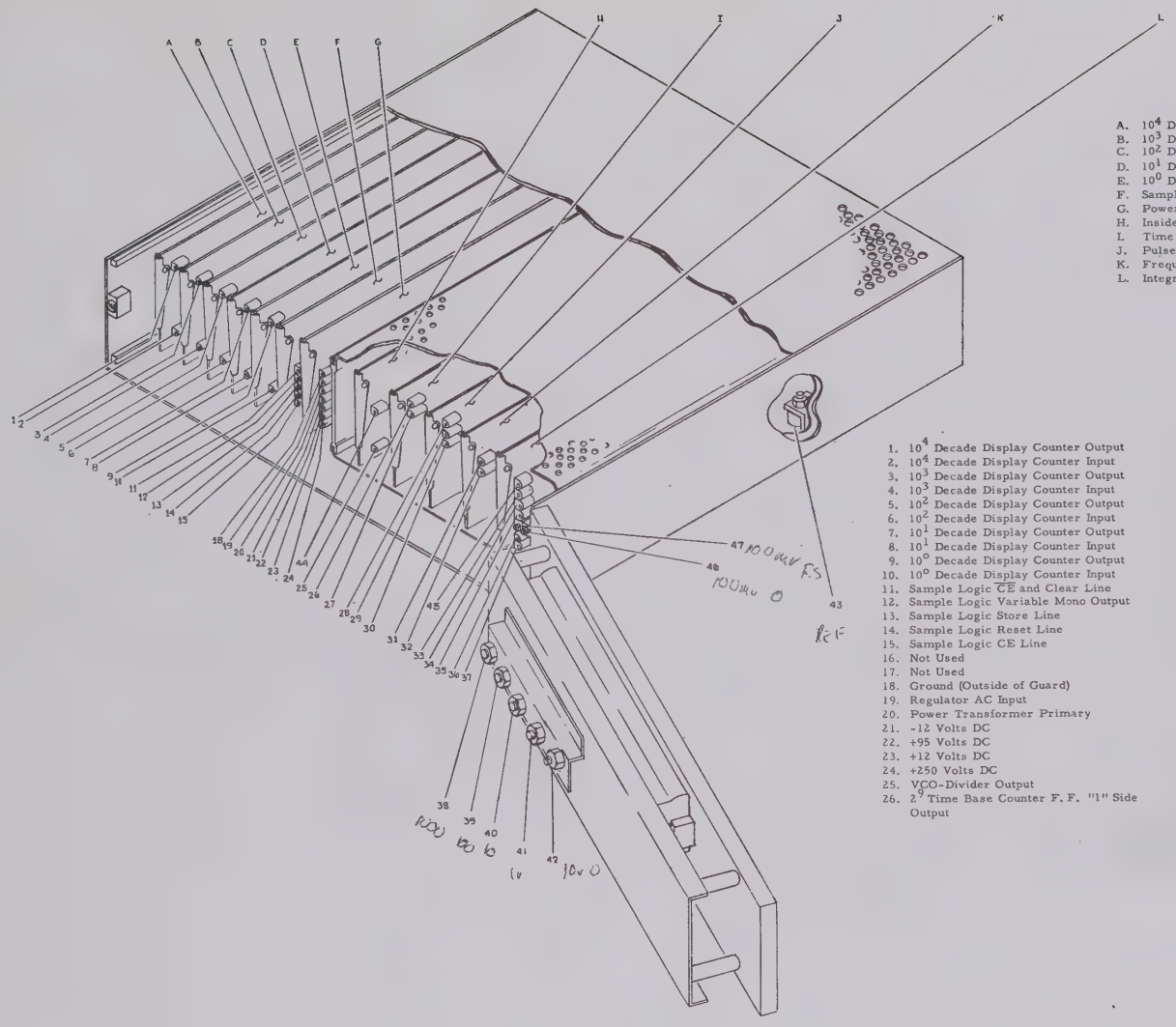
e. Adjust output of voltage standard to +99. 999 millivolts.

f. With front panel service door open observe display and adjust the 100 millivolt range control on intergrator amplifier board 104-129 (47, figure 4. 1) for a reading of +99. 999 millivolts.

NOTE

All ranges are affected by the setting of the 100 millivolt calibration control. For this reason the 100 millivolt range is calibrated first.

g. Increase output of voltage standard to +999. 99 millivolts. Then set RANGE switch on Model 630 to 1000MV position.



A. 10^4 Decade Display Counter 104-118
B. 10^3 Decade Display Counter 104-118
C. 10^2 Decade Display Counter 104-118
D. 10^1 Decade Display Counter 104-118
E. 10^0 Decade Display Counter 104-116
F. Sample Logic Board 104-121
G. Power Supply and AC Regulator Board 104-104
H. Inside Power Supply Board 104-125
I. Time Base Board 104-124
J. Pulse Generator Board 104-126
K. Frequency Board 104-127
L. Integrator Amplifier Board 104-129

1. 10^4 Decade Display Counter Output
2. 10^4 Decade Display Counter Input
3. 10^3 Decade Display Counter Output
4. 10^3 Decade Display Counter Input
5. 10^2 Decade Display Counter Output
6. 10^2 Decade Display Counter Input
7. 10^1 Decade Display Counter Output
8. 10^1 Decade Display Counter Input
9. 10^0 Decade Display Counter Output
10. 10^0 Decade Display Counter Input
11. Sample Logic $\overline{CE}$ and Clear Line
12. Sample Logic Variable Mono Output
13. Sample Logic Store Line
14. Sample Logic Reset Line
15. Sample Logic CE Line
16. Not Used
17. Not Used
18. Ground (Outside of Guard)
19. Regulator AC Input
20. Power Transformer Primary
21. -12 Volts DC
22. +95 Volts DC
23. +12 Volts DC
24. +250 Volts DC
25. VCO-Divider Output
26. 2^9 Time Base Counter F. F. "1" Side Output
27. Time Base F. F. "1" Side Output
28. 2^7 Time Base Counter F. F. "1" Side Output
29. Pulse Width F. F. "1" Side Output
30. Ground (Inside Guard)
31. Frequency Amplifier Output
32. Schmitt Circuit Output
33. Correction Amplifier Output
34. -12 Volts DC
35. Ground (Inside Guard)
36. Wide Band Amplifier Output
37. VCO Output
38. 750 Volt Range Calibration Adjustment
39. 100 Volt Range Calibration Adjustment
40. 10 Volt Range Calibration Adjustment
41. 1 Volt Range Calibration Adjustment
42. Zero Calibration Adjustment For 10 Volt Range
43. Reference Supply Zener Current Calibration Adjustment
44. Correction Amplifier Chopper Drive
45. +12 Volts DC
46. Zero Calibration Adjustment for 100 mv Range
47. 100 Millivolt Range Calibration Adjustment

Figure 4.1. Model 630, Test Points and Calibration Adjustments

h. Observe front panel display and adjust 1V range control on rear of front panel for a reading of +999.99 millivolts.

i. Set RANGE switch on Model 630 to 10V position and increase output of voltage standard to +9.9999 volts.

j. Observe front panel display and adjust 10V range control on back side of service door (40, figure 4.1) for a reading of +9.9999 volts.

k. Set RANGE switch on Model 630 to 100V position and increase output of voltage standard to +99.999 volts.

l. Observe front panel display and adjust 100V range control (39, figure 4.1) for a reading of +99.999 volts.

m. Set RANGE switch on Model 630 to 750V position and adjust output of voltage standard to +750.00 volts.

n. Observe front panel display and adjust 750V range control (38, figure 4.1) for a reading of +750.00.

NOTE

It is suggested that both polarities and a number of points within each range be checked.

4.1.4 Zener Current Adjustment (For replacement Zener only)

NOTE

The following procedures are to be followed when a replacement 1N931 Zener is being installed in the reference bridge circuit on inside power supply board 104-125.

a. Leave one lead on new Zener unsoldered and connect milliammeter (0 to 10 ma) in series with the Zener and the unsoldered Zener terminal on the board.

CAUTION

In following these procedures do not allow Zener to overheat. Failure to observe this rule will cause the Zener characteristics to change and prevent proper meter calibration.

b. Install the power supply board into its proper connector and plug the AC power cable into appropriate AC power source.

c. Set POWER switch to ON and allow at least 15 minutes for warmup.

d. Remove the top cover from instrument and adjust the reference Zener current control (43, figure 4.1) until the milliammeter reads the current value specified for the new Zener by Electro Instruments, Inc.

e. Set POWER switch to OFF.

f. Remove the power supply board from instrument and disconnect milliammeter from circuit. Solder disconnected Zener lead to proper terminal on board, taking care not to overheat Zener.

g. Install power supply board back into instrument and perform zero offset and range calibration adjustments given in paragraph 4.2.2 and 4.2.3.

SECTION V

MAINTENANCE

5.1 GENERAL

When used within the limits specified, and with reasonable care, the Electro Instruments' Model 630 Digital Voltmeter should have a useful life measured in years. Because of the solid state circuit design of the instrument and the logic with which the physical design is associated, trouble analysis and repair can be simply and quickly accomplished.

5.2 PREVENTIVE MAINTENANCE

Preventive maintenance of the Model 630 consists primarily of periodic inspection and dust removal.

5.3 TROUBLE ISOLATION

Tables 5.1, 5.2, and 5.3 may be used to aid in isolating trouble. To use the information provided, first consult the column headed "Symptom" until an observed condition is recognized. Next consult the successive right-hand columns for the probable cause of the trouble and the appropriate check-out procedure. The information given is based on factory service experience. Other troubles may occur that will require signal tracing techniques. In this event, standard procedures are acceptable except as noted herein. Typical waveforms to be expected at various test points during the sample logic sequence are shown in figure 5.1 and are referred to in the trouble isolation charts. A further aid for isolating trouble is provided by table 5.4 in which are listed all plug-in etched circuit boards and their functions. (Refer to figure 4.1 for circuit board layout.)

When the checkout procedures in table 5.1 are used the meter controls should be set to continuous encode, 1000 millivolt range, and the HI, LO, and GUARD input terminals should be shorted together.

Table 5.1. Trouble Isolation Chart, DC Voltage Mode

SYMPTOM	PROBABLE CAUSE	CHECKOUT PROCEDURE
1. Meter is inoperative and readout does not light.	a. Line voltage not present.	a. Check power cable, and power source fuse or circuit breaker.
	b. Blown line fuse in instrument.	b. Check fuses on rear panel.

SYMPTOM	PROBABLE CAUSE	CHECKOUT PROCEDURE
1. (Continued)	c. Defective 2N1159 AC series regulator transistor or diode rectifier in power supply.	c. Check 2N1159 transistor mounted adjacent to power transformer at right rear of chassis. Check for shorted voltage supplies on boards 104-104 and 104-125 (G and H, figure 4.1).
2. Meter operates but readout is blurred	a. ENCODE switch in REMOTE position	a. Set ENCODE switch to CONT position or rotate to SINGLE ENCODE position.
	b. Sample logic loop inoperative	b. Check red test point (10, fig. 4.1) on end of 10^{o} display counter board 104-116 for a series of pulse trains (Waveform G, Fig. 5.1). If pulse trains are not present: (1) Check point 26, fig. 4.1 on time base board 104-124 for 0-volts indicating that 2^{9} flip-flop (Q42, Q43) is in set state (See waveform B, fig. 5.1); (2) Check pin 12 on board 104-125 to see that display multivibrator is oscillating at nominal 500 cps; (3) Check for presence of pulse at each test point on end of board 104-121 to see if sample logic sequencer is going through cycle(waveforms I, J, K, L, M, and N, fig. 5.1) upon receipt of pulses from display multivibrator on inside power supply board (Refer to paragraph 3.5.1); (4) Check to see that sample logic circuit is sending a pulse (waveform A, fig. 5.1) to the reset input of

Table 5.1. Trouble Isolation Chart, DC Voltage Mode (Continued)

SYMPTOM	PROBABLE CAUSE	CHECKOUT PROCEDURE
2. (Continued)		b. (Continued) the 2^9 flip-flop on time base board 104-124 (connector terminal 10) at end of each display and storage cycle when green test point on board 104-121 changes to ground potential; (5) Check to see that 2^9 flip-flop resets (goes to ground at test point 26, fig. 4.1) upon receipt of pulse from sample logic; (6) Check to see that reset state of 2^9 flip-flop enables dynamic AND gate at pin 8 board 104-124 and allows a spike from VCO divide-by 64 counter on board 104-125 to pass through gate at pin 8 and set time base flip-flop (Q1, Q2). (See waveforms B, C, and D on fig. 5.1.)
3. Readout locks at 19999 when FUNCTION switch is set to VOLT 0.1 sec sample, or at 99999 when FUNCTION switch is set to VOLT 1-sec sample	a. Sample logic loop inoperative. b. VCO not oscillating	a. See 3b above. b. Check for VCO signal at orange test point on end of board 104-129 (35, fig. 4.1). If signal is not present as shown for waveform E in fig. 5.1, check red test point (33, fig. 4.1) for proper output from chopper amplifier as shown for TP1 on integrator amplifier schematic. Then check yellow test point (36, fig. 4.1) for proper DC voltages at output

Table 5.1. Trouble Isolation Chart, DC Voltage Made (Continued)

SYMPTOM	PROBABLE CAUSE	CHECKOUT PROCEDURE
3. (Continued)		b. (Continued) of wide-band amplifier as shown for TP4 on integrator amplifier schematic.
4. Meter is unstable and error lamp lights, indicating overrange.	a. Feedback loop around integrator amplifier not functioning.	a. Check orange test point (37, fig. 4.1) on end of board 104-129 for signal out of VCO as shown for waveform E in fig. 5.1. Check brown test point on board 104-125 for VCO divide-by 64 counter output signal (Waveform D, fig. 5.1). Check yellow test point 29 (fig. 4.1) on one end of board 104-126 for pulses having 180 μsec duration and same frequency as signal at red test point on board 104-125. Check collector of Q13 in precision flip-flop on board 104-129 for waveform similar to that at the yellow test point on end of board 104-126.
5. Meter is unstable.	a. Pulse width generator not functioning properly.	a. Synchronize oscilloscope to leading edge of positive pulse at yellow test point (29, fig. 4.1) on end of board 104-126 so as to eliminate all visible jitter at leading edge. Set scope horizontal sweep at 20 μsec/cm. Check for pulse width of 180 μsec. Then expand horizontal sweep on scope to x 20. Check that no visible jitter is present at trailing

Table 5.1. Trouble Isolation Chart, DC Voltage Mode (Continued)

SYMPTOM	PROBABLE CAUSE	CHECKOUT PROCEDURE
5. (Continued)		a. (Continued) edge of pulse. If pulse has jitter or a duration other than 180 μsec, or is not present, check following: (1) the yellow test point (29, fig. 4.1) on end of board 104-126 should go positive when the P. W. flip-flop Q2, Q3 is triggered by the VCO divider (waveform D, fig. 5.1); (2) Each of the pulse width counter flip-flops (2^0 through 2^7) on board 104-126 should divide its input frequency by a factor of 2 during the time the yellow test point on end of pulse generator board 104-126 is positive; (3) 180 μsec after the yellow test point on end of board 104-126 goes positive, AND gate at reset input to pulse width flip-flop should go positive at its output terminal (junction of R1 & C1) for 1/2 microsecond; (4) Negative-going trailing edge of output pulse from this AND gate should reset P. W. flip-flop (switch the level to 0 volts at the yellow test point on end of board 104-126).
	b. Chopper amplifier is inoperative or saturated.	b. Check signal at red test point (33, fig. 4.1) on end of integrator amplifier board 104-129. If signal

Table 5.1. Trouble Isolation Chart, DC Voltage Mode (Continued)

SYMPTOM	PROBABLE CAUSE	CHECKOUT PROCEDURE
5. (Continued)		b. (Continued) is a square wave greater than 2 volts peak-to-peak, or is dissimilar from the waveform shown for test point TP2 on the integrator amplifier schematic, check following: (1) that none of transistor stages on board is saturated or cut off; (2) that, with a signal present on the grid of V1, each common emitter stage provides some gain and signal inversion.
	c. Ripple in power supply	c. Check that -12 volt supply at pin 30 on board 104-129 has no more than 30 millivolts P-P of ripple. Check +12 volts supply at blue test point to be sure that no more than 30 millivolts P-P is present. Check +40 volt supply at pin 4 to be sure that no more than 1 millivolts P-P ripple is present.
6. Meter is stable and linear but cannot be calibrated to specifications	a. Duration of pulse out of P. W. flip-flop at pin 20 on pulse generator board 104-126 too short or too long.	a. Check pulse width generator as described in step 5a above.
	b. Integrator amplifier input or feedback resistors on board 104-129 and on back of front panel shorted or partially open.	b. Check to see that resistors R8, R9, R12, R13, R28, R30, R127 are in tolerance.

Table 5.1. Trouble Isolation Chart, DC Voltage Mode (Continued)

SYMPTOM	PROBABLE CAUSE	CHECKOUT PROCEDURE
6. (Continued)	c. Defective 1N938 Zener diode on board 104-125.	c. Check for approximately 9.0 volts between pins 17 and 10 on board 104-125
	d. Time base generator not operating correctly.	d. Synchronize oscilloscope to leading edge of positive time base pulse(waveform C, fig. 5.1) at red test point 27 on board 104-124 so as to eliminate visible jitter at leading edge. Set horizontal sweep at 10 milliseconds. If pulse width is incorrect, has jitter, or no pulse is present, check the following: (1) red test point 27 on board 104-124 should go positive(waveform C, fig. 5.1) when T.B. flip-flop is triggered by output of VCO divide-by 64 counter on board 104-125(waveform D, fig. 5.1); (2) the first four flip-flops(Q4 through Q11) in time base counter chain should count down without error the 1 MC frequency at pin 17 to 100 KC at pin k when the red test point on board 104-124 is positive; (3) the second four flip-flops (Q12 through Q19) in time base counter chain should count down without error the 100 KC frequency at pin k to 10 KC at pin F when the red test point on board 104-124 is positive; (4) each of the time base counter flip-flops 2^0

Table 5.1. Trouble Isolation Chart, DC Voltage Mode (Continued)

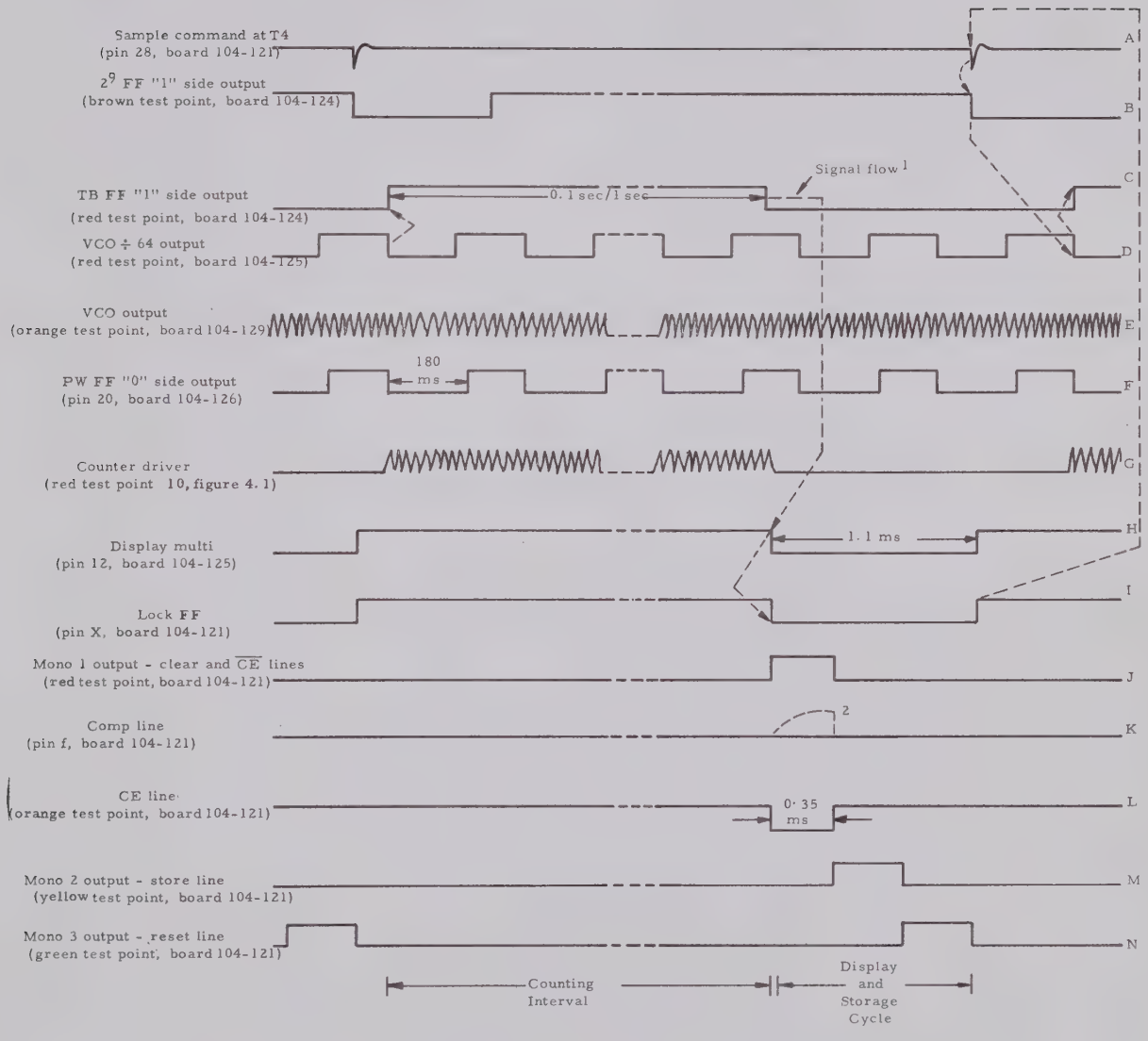
SYMPTOM	PROBABLE CAUSE	CHECKOUT PROCEDURE
6. (Continued)		d. (Continued) through 2^{13} should divide down without error by a factor of 2 the frequency at its input during time the red test point on board 104-124 is positive; (5) 100 milliseconds after the TB flip-flop sets(waveform C, fig. 5.1), AND gate at pin 18 should go positive for 1/2 microsecond; (6) negative going trailing edge of pulse out of aforementioned AND gate should reset TB flip-flop and make red test point on board 104-124 switch to 0 volts.
7. Meter is stable and linear but offset cannot be adjusted out	a. Pulse out of P.W. flip-flop either too short or too long.	a. Check pulse width generator as in step 5a above.
	b. Reference divider resistors out of tolerance	b. Check resistors R15 and R21 on board 104-125.
	c. Chopper amplifier not operating correctly.	c. Check chopper amplifier on board 104-129 as in step 5b above.
	d. Time base generator not operating correctly.	d. Check time base generator as in step 6d above.
	e. Display counters not counting correctly.	e. Check, in sequence, the pulse frequency at the red test points(10, 8, 6, 4, 2, fig. 4.1) on end of 10^0, 10^1, 10^2, 10^3, and 10^4 display counters(boards 104-116, 104-118). Then check the brown test point (1, fig. 4.1) on the 10^4

Table 5.1. Trouble Isolation Chart, DC Voltage Mode (Continued)

SYMPTOM	PROBABLE CAUSE	CHECKOUT PROCEDURE
7. (Continued)		e. (Continued) display counter board (A, fig. 4.1). In each case the pulse frequency observed should be 1/10 of previous test point.
	f. Display counters not resetting correctly.	f. Check to see that all counting flip-flops on 10^0, 10^1, 10^2, and 10^3 display counter boards(D, C, B, and E, fig. 4.1) are resetting to their 0 states at end of storage cycle (pins 14, 16, 18, and 20 on each board should go positive). In the 10^4 display counter(A, fig. 4.1), pins 14, 17, 19, and 21 should go positive at end of storage cycle in 0.1 second sample mode. In 1 second sample mode pins 14, 16, 18, and 20 should go positive. To facilitate this check set ENCODE switch to VAR position and adjust variable ENCODE rate control to approximately 1 second/sample.
8. Meter is stable but non-linear.	a. Operational amplifier gain too low.	a. Check for leakage in feedback diodes CR13, CR14, CR26, and CR27 on board 104-129(L, fig. 4.1). Check each stage for gain in chopper amplifier. Check each stage for gain in wide-band amplifier.

Table 5.1. Trouble Isolation Chart, DC Voltage Mode (Continued)

SYMPTOM	PROBABLE CAUSE	CHECKOUT PROCEDURE
9. One numeral stays on in readout or does not light.	a. Associated storage circuit inoperative.	a. Check clear line (red test point 11, fig. 4.1) store line (yellow test point 13, fig. 4.1) and reset line (green test point 14, fig. 4.1) on end of board 104-121 for correct waveforms, as illustrated in fig. 5.1 for waveforms J, M, and N, respectively. Check that storage circuit associated with numeral locked in readout is receiving above pulses. Check for defective Nixie driver transistor.
	b. Defective Nixie lamp.	b. Check by switching with adjacent lamp.
10. All numerals in readout light, or none light.	a. Sample logic waveforms incorrect.	a. Check test points 11, 12, 13, 14, 15 on end of board 104-121 (F, fig. 4.1) for correct waveforms during storage and display cycle. Also check to see that each test point remains at correct voltage level during counting interval (see fig. 5.1, waveforms J, K, L, M, and N).
11. Meter will not measure negative voltages but measures positive voltages correctly.	a. Display counters not complementing during storage and display cycle.	a. Check that complement (comp) pulse appears at correct time at pin f on end of board 104-121 (see fig. 5.1, waveform K).



1. The dotted line represents the flow of sample logic signal from point to point.
2. Comp pulse appears only for negative voltage measurement.

Figure 5.1. Sample Logic Waveforms

Table 5.2. Trouble Isolation Chart, Frequency Mode (Continued)

Symptom	Probable Cause	Suggested Remedy
2. Continued.		end of board 124-125 goes positive for an instant at end of each 10 second interval. (Refer to paragraph 3.7.1.)

Table 5.3. Trouble Isolation Chart, Period/Time Interval Mode

Symptom	Probable Cause	Suggested Remedy
1. Meter reads a constant value unrelated to period or time interval being measured.	a. Selected slope of input waveform does not cross zero axis.	a. Apply input waveform to HI input terminal through blocking capacitor, or offset the input signal so selected slope of waveform does pass through zero axis.
	b. Schmitt circuit on frequency board 104-127 not being triggered by input waveform.	b. Check ENABLE gate CR9, R16 and OR gate CR11, CR12, CR13, R18 on frequency board 104-127 to see if applied waveform is passing through these gates from output of wideband amplifier on integrator amplifier board 104-129.
	c. Waveform at output of Schmitt circuit on frequency board 104-127 not passing through appropriate slope selection gates on frequency board 104-127 or input gate to the time base flip-flop on time base board 104-124.	c. Refer to paragraph 3.8 and figure 3.12.
2. Meter reading is approximately correct but out of specified tolerance	Crystal controlled oscillator Q5 on pulse generator board 104-126 out of tolerance.	Measure frequency of oscillator at pin 27 of pulse generator board. Replace crystal if frequency is less than 999.90 KC or greater than 1000.10 KC.

Table 5.3. Trouble Isolation Chart, Period/Time Interval Mode (Continued)

Symptom	Probable Cause	Suggested Remedy
3. Measurements are correct when using 0.1 second time base but incorrect when using 1 second time base.	Time base counter on time base board 104-124 not supplying 100 KC pulses to display counter during sample period.	Check pin k on time base board for presence of 100 KC pulses during time red test point on board is positive. If absent, check first four stages of time base counter (Q4 through Q11) to see if these are dividing 1 megacycle clock frequency down to 100 KC.
4. Measurements are correct when using 0.1 second and 1 second time bases but incorrect when using 10 second time base.	Time base counter on time base board 104-124 not supplying 10 KC pulses to display counter during sample period.	Check pin F on time base board for presence of 10 KC pulses during sample period. If absent, check flip-flops (Q12 through Q19) to see if these are dividing 100 KC pulses (at pin k) down to 10 KC.

Table 5.4. Printed Circuit Boards and Their Functions

NAME OF BOARD	NUMBER	FUNCTION
10^4 Decade Display Counter	104-118	a. Counts the carry-over pulses produced by the 10^3 decade during the sampling period. b. Produces a carry-over pulse after each ten counts to step the polarity and error counter on the sample logic board if a 1-second or 10-second time base is being used for the sampling period. c. Converts the final count for the 10^4 digit of measurement from binary code to its decimal equivalent. d. Converts the decimal equivalent of the 10^3 digit of measurement to its nines complement if a negative-DC voltage is being measured. e. Drives the Nixie indicator representing the 10^4 digit of measurement in the read-out and provides corresponding logic levels of 0 and +70 volts to an output connector on the 10^4 digit line.
10^3 Decade Display Counter	104-118	a. Counts in ten steps from 0 through 9 the carry over pulses produced by the 10^2 decade display counter. b. Supplies a carry-over pulse after each ten counts to step the 10^4 decade display counter and also to step the polarity and error counter on the sample logic board if a 1-second time base is being used for the sample period. c. Converts the final count for the 10^3 digit of measurement from binary code to its decimal equivalent. d. Converts the decimal equivalent of the 10^3 digit to its nines complement if a negative DC voltage is being measured. e. Drives the Nixie indicator representing the 10^3 digit of measurement in the read-out and provides corresponding logic levels of 0 and +70 volts to an output connector on the 10^3 digit line.

Table 5.4. (Continued)

NAME OF BOARD	NUMBER	FUNCTION
10^2 Decade Display Counter	104-118	a. Counts in ten steps from 0 through 9 the carry pulse produced at every tenth count by the 10^1 decade display counter. b. Supplies a carry pulse after each ten counts to step the 10^3 decade display counter . c. Converts the final count for the 10^2 digit of measurement from binary code to its decimal equivalent. d. Converts the decimal equivalent to its nines complement if a negative DC voltage is being measured. e. Drives the Nixie indicator representing the 10^2 digit of measurement in the readout and provides corresponding logic levels of 0 and +70 volts to an output connector on the 10^2 digit line.
10^1 Decade Display Counter	104-118	a. Counts in ten steps from 0 through 9 the carry pulses produced by the 10^0 decade display counter. b. Supplies a pulse after each ten counts to step the 10^2 decade display counter. c. Converts the final count for the 10^1 digit of measurement from binary code to its decimal equivalent. d. Converts the final count for the 10^1 digit of measurement to its nines complement if a negative DC voltage is being measured. e. Drives the Nixie indicator representing the 10^1 digit of measurement in the readout and provides corresponding logic levels of 0 and +70 volts to an output connector on the 10^1 digit line.
10^0 Decade Display Counter	104-116	a. Counts in ten steps from 0 through 9 the pulses from either the VCO, frequency amplifier, or time base divider during the sampling period.

Table 5.4. Printed Circuit Boards and Their Functions

NAME OF BOARD	NUMBER	FUNCTIONS
10^0 Decade Display Counter (Continued)	104-116	b. Supplies a pulse after each ten counts to step the 10^1 decade display counter. c. Converts the final count for the 10^0 digit of measurement from binary code to its decimal equivalent. d. Converts the final count for the 10^0 digit of measurement to its nines complement if a negative DC voltage is being measured. e. Drives the Nixie indicator representing the 10^0 digit of measurement in the readout and provides corresponding logic levels of 0 and +70 volts to an output connector on the 10^0 digit line.
Sample Logic	104-121	a. Supplies enabling signals to control the storage and display sequence. b. Supplies a pulse at the end of the storage and display cycle to activate time base counter. c. Determines DC polarity and overrange and controls polarity and overrange indicators in readout.
Power Supply and AC Regulator	104-104	a. Regulates AC voltage across power supply transformer primary to counteract line and load variations. b. Supplies DC voltages of 12 volts, 70 volts 95 volts, 250 volts, and -2 volts for circuits outside of guard.
Inside Power Supply	104-125	a. Supplies +14 volts and -14 volts DC and +45 volts DC for circuits inside guard. b. Supplies 9.0 volt floating reference to precision flip-flop circuit on integrator amplifier during DC voltage measurements.

Table 5.4. Printed Circuit Boards and Their Functions

NAME OF BOARD	NUMBER	FUNCTIONS
Inside Power Supply (Continued)	104-125	c. Supplies pulses to sample logic board at end of each sampling period to start display and storage cycle. d. Divides VCO output frequency during DC voltage measurements by a factor of 64 to trigger 180 microsecond pulse width counter on pulse generator board. e. Provides last three divide-by-2 stages of time base counter on frequency 10-second sample period.
Time Base	104-124	a. Supplies enabling pulses having durations of either 0.1 second, 1 second, or 10 seconds to enable input gate to display counter during sampling period in voltage or frequency mode. b. Supplies either 10 KC, 100 KC, or 1 MC pulses which are counted by the display counter on period and time interval measurements.
Pulse Generator	104-126	a. Supplies 1 MC reference for time base and pulse width counters. b. Supplies pulses to trigger precision flip-flop circuit on integrator amplifier board during DC voltage measurements. The pulses have duration of 180 microseconds and a frequency which is directly proportional to the input voltage and range from 1550 CPS to 4650 CPS.
Frequency Board	104-127	a. Gates pulses from either the VCO, frequency amplifier, or time base counter to the display counter for counting during sampling period. b. Converts to rectangular waveform the applied signal being measured for period or time interval.

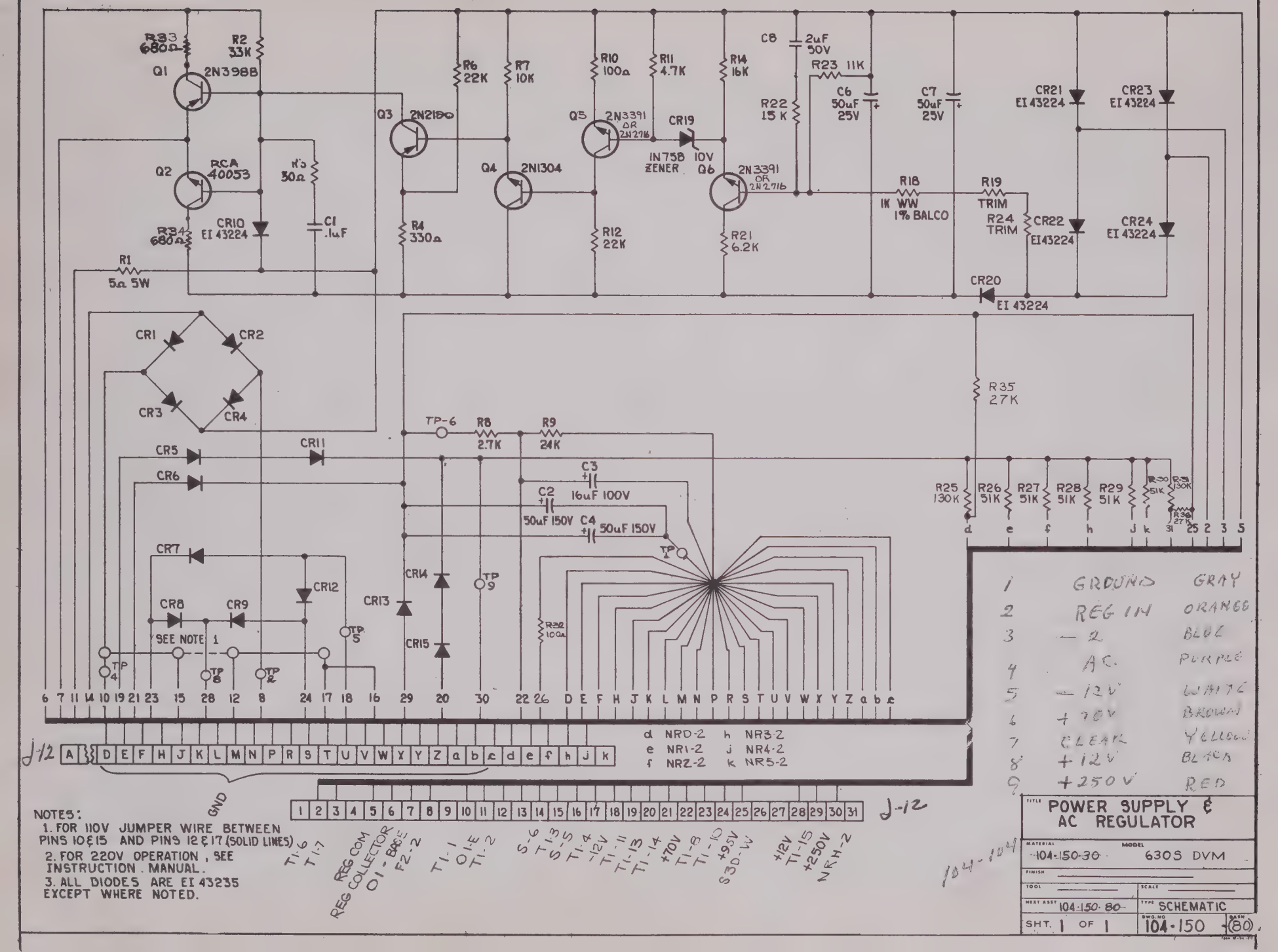
Table 5.4. Printed Circuit Boards and Their Functions

NAME OF BOARD	NUMBER	FUNCTIONS
Frequency Board (Continued)	104-127	c. Provides four divide-by-2 stages of time base counter during 1 second and 10 second sample period. d. Shapes the input frequency waveform during frequency measurements into a rectangular waveform of constant amplitude before it is applied to the display counter for counting. e. Shapes the VCO output pulses during DC voltage measurements into a rectangular waveform of constant amplitude before application to the display counter for counting.
Integrator Amplifier	104-129	a. Converts input signal on DC voltage measurements into a pulse waveform having a frequency that is directly proportional to a positive input. b. Provides amplification or limiting on input waveforms for period and time interval measurement.

MODEL 630

DRAWING LIST

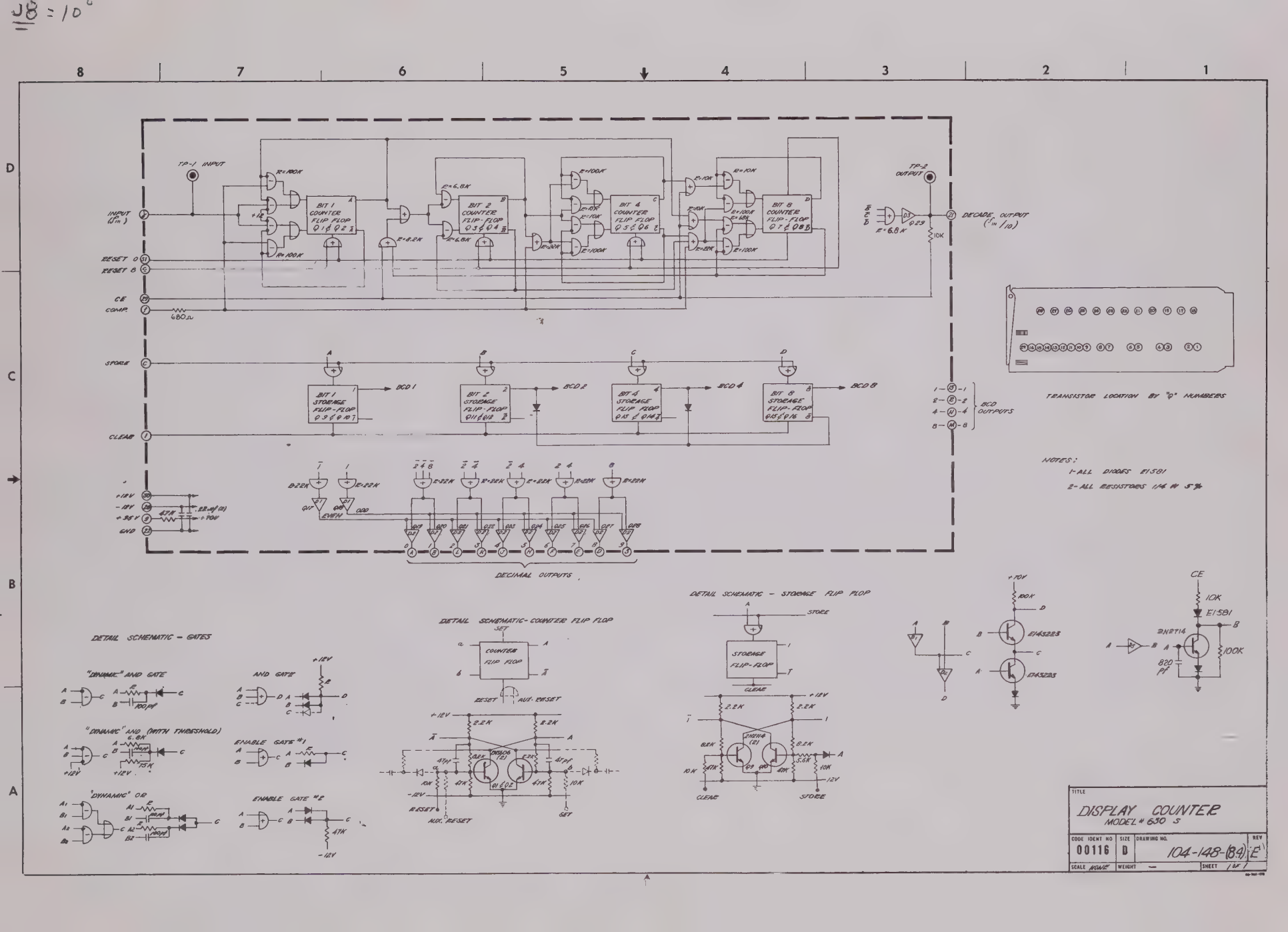
Nomenclature	Schematic
Power Supply and AC Reg. Board	104-150
Decade Board	104-148
Sample Logic Board	104-136
Time Base Board	104-124
Inside Power Supply Board	104-155
Precision Reference Supply RS-9	104-156
Pulse Generator Board	104-126
Frequency Board	104-127
Integrator Amplifier Board	104-129
Inside Wiring Diagram	104-131
Outside Wiring Diagram	104-132

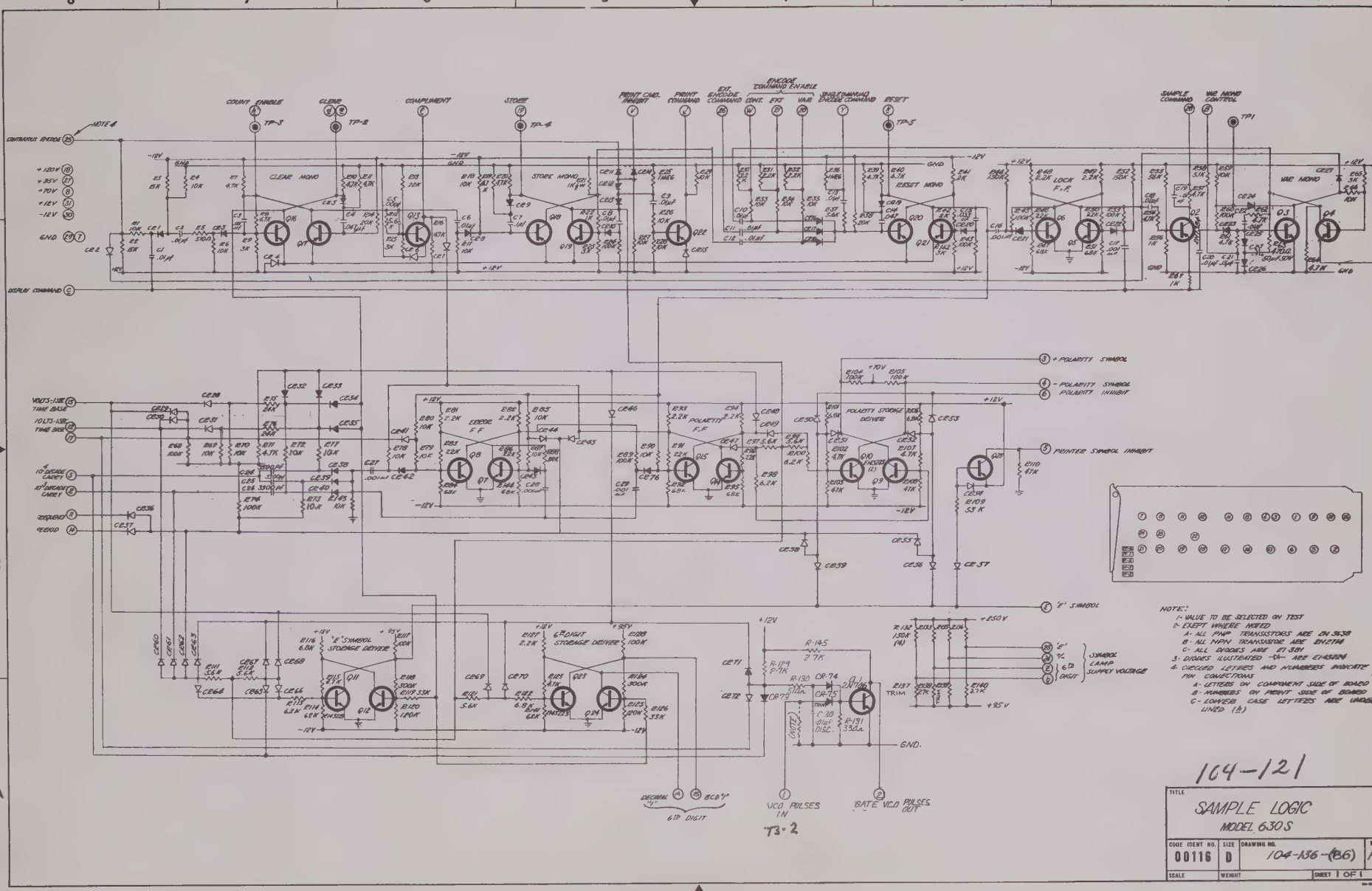


NOTES:
1. FOR 110V JUMPER WIRE BETWEEN PINS 10 & 15 AND PINS 12 & 17 (SOLID LINES)
2. FOR 220V OPERATION, SEE INSTRUCTION MANUAL.
3. ALL DIODES ARE EI 43235 EXCEPT WHERE NOTED.

104-104

TITLE	POWER SUPPLY & AC REGULATOR
MATERIAL	104-150-30
MODEL	630S DVM
FINISH	
TOOL	
SCALE	
NEXT ASSY	104-150-80
TYPE	SCHEMATIC
SHT. 1 OF 1	
DWG. NO.	104-150
REV	(80)

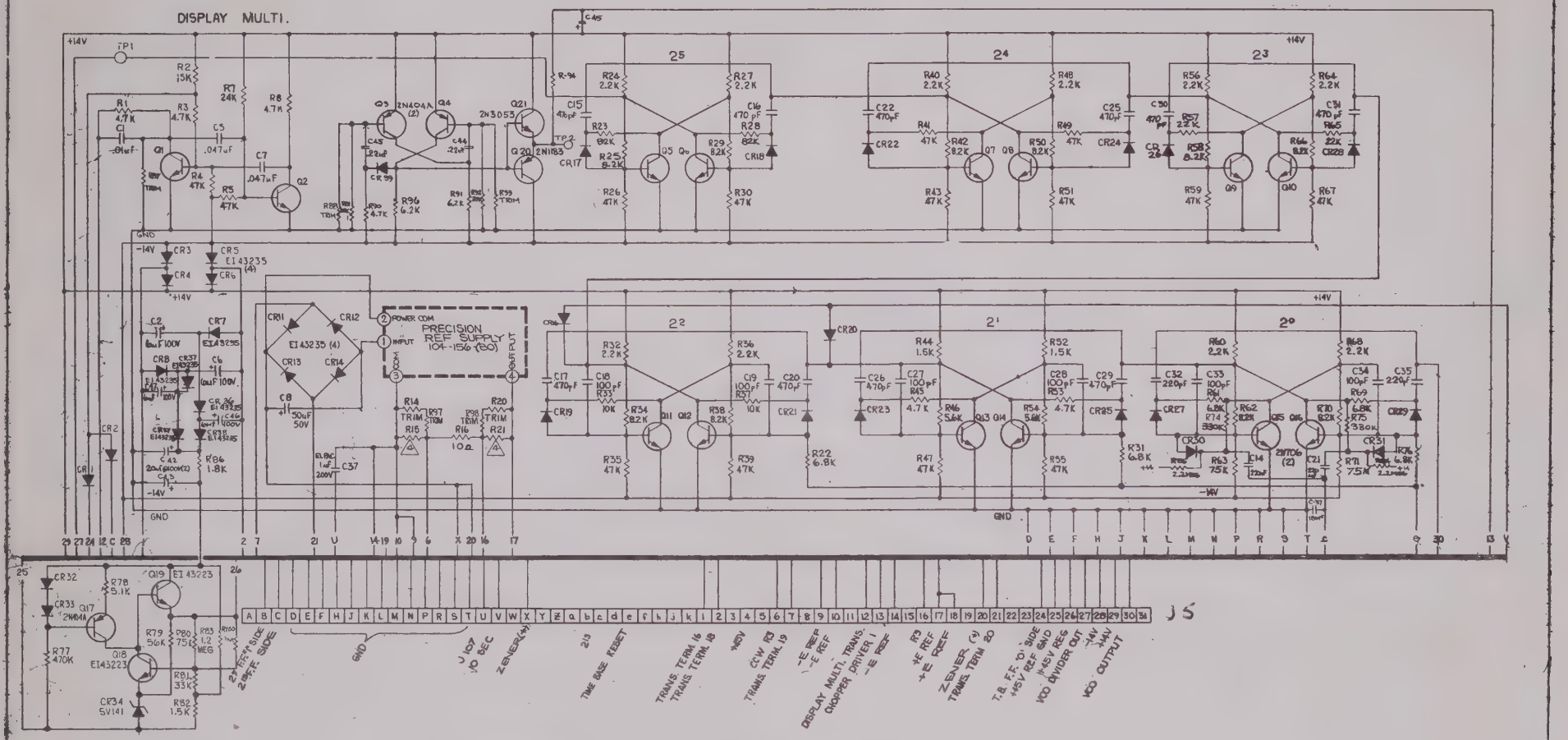

TP-1 INPUT
TP-2 OUTPUT
INPUT (f_{in})
RESET 0
RESET B
CE
COMP.
680Ω
BIT 1 COUNTER FLIP FLOP Q1 & Q2
BIT 2 COUNTER FLIP-FLOP Q3 & Q4
BIT 4 COUNTER FLIP FLOP Q5 & Q6
BIT 8 COUNTER FLIP-FLOP Q7 & Q8
DECADE OUTPUT (f_{in} / 10)
STORE
CLEAR
BIT 1 STORAGE FLIP-FLOP Q9 & Q10
BIT 2 STORAGE FLIP-FLOP Q11 & Q12
BIT 4 STORAGE FLIP FLOP Q13 & Q14
BIT 8 STORAGE FLIP-FLOP Q15 & Q16
BCD 1
BCD 2
BCD 4
BCD 8
BCD OUTPUTS
+12V
-12V
+5V
GND
EVEN
ODD
DECIMAL OUTPUTS
TRANSISTOR LOCATION BY "Q" NUMBERS
NOTES:
1- ALL DIODES E1581
2- ALL RESISTORS 1/4 W 5%
DETAIL SCHEMATIC - GATES
"DYNAMIC" AND GATE
"DYNAMIC" AND (WITH THRESHOLD)
"DYNAMIC" OR
AND GATE
ENABLE GATE #1
ENABLE GATE #2
DETAIL SCHEMATIC - COUNTER FLIP FLOP
COUNTER FLIP FLOP
SET
RESET
AUT. RESET
NOR. RESET
DETAIL SCHEMATIC - STORAGE FLIP FLOP
STORAGE FLIP-FLOP
CLEAR
STORE
2N2714
E143223
E1581
TITLE
DISPLAY COUNTER
MODEL # 630 S
CODE IDENT NO 00116
SIZE D
DRAWING NO. 104-148-(B4)
REV E
SCALE NONE
WEIGHT
SHEET 1 OF 1



NOTE:
1- VALUE TO BE SELECTED ON TEST
2- EXCEPT WHERE NOTED
A- ALL PNP TRANSISTORS ARE 2N 3638
B- ALL NPN TRANSISTOR ARE 2N2714
C- ALL DIODES ARE #1 38?
3- DIODES ILLUSTRATED → ARE 1N4152M
4- CIRCLED LETTERS AND NUMBERS INDICATE PIN CONNECTIONS
A- LETTERS ON COMPONENT SIDE OF BOARD
B- NUMBERS ON PRINT SIDE OF BOARD
C- LOWER CASE LETTERS ARE UNDERLINED (a)

104-121

TITLE			
SAMPLE LOGIC MODEL 630S			
CODE IDENT NO. 00116	SIZE D	DRAWING NO. 104-136-(B6)	REV F
SCALE	WEIGHT	SHEET 1 OF 1	

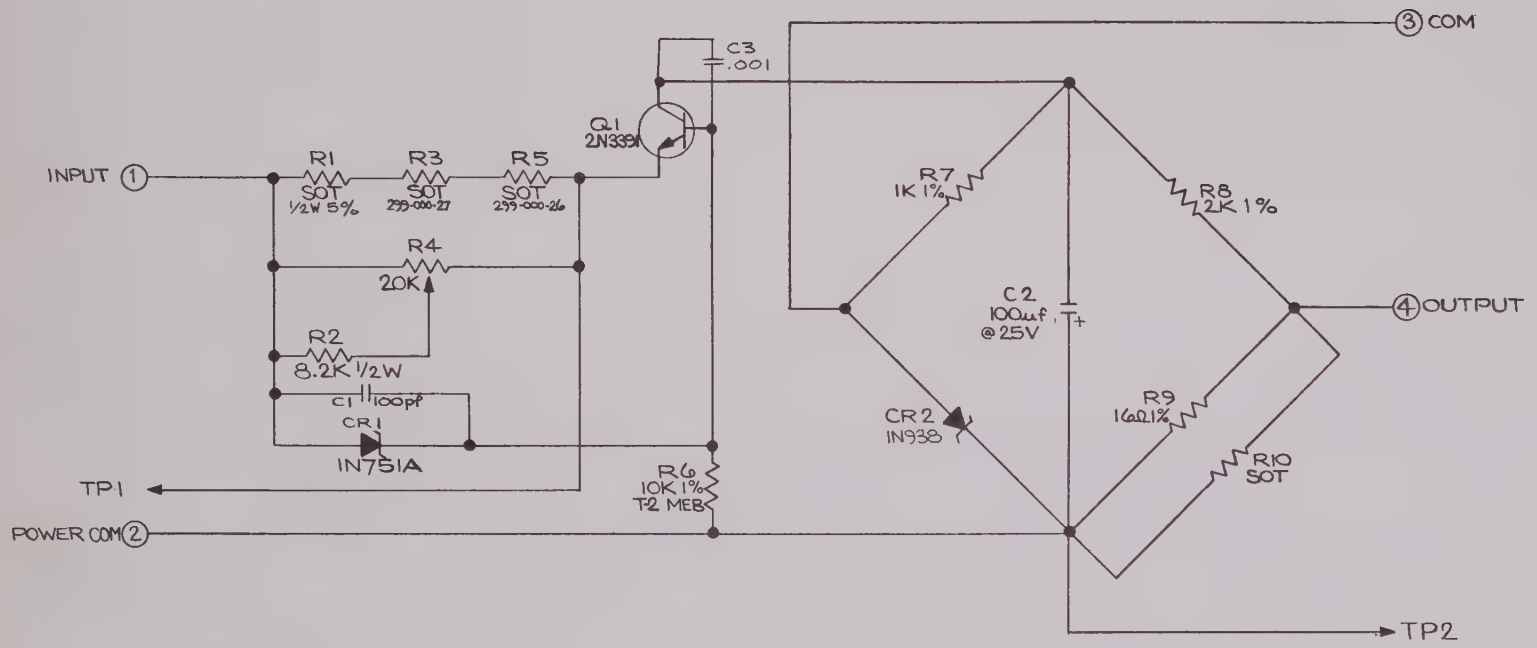


CHOPPER	RESISTOR	CAPACITOR
JAMES C-2705	R94 150Ω	C45 22uf 50V

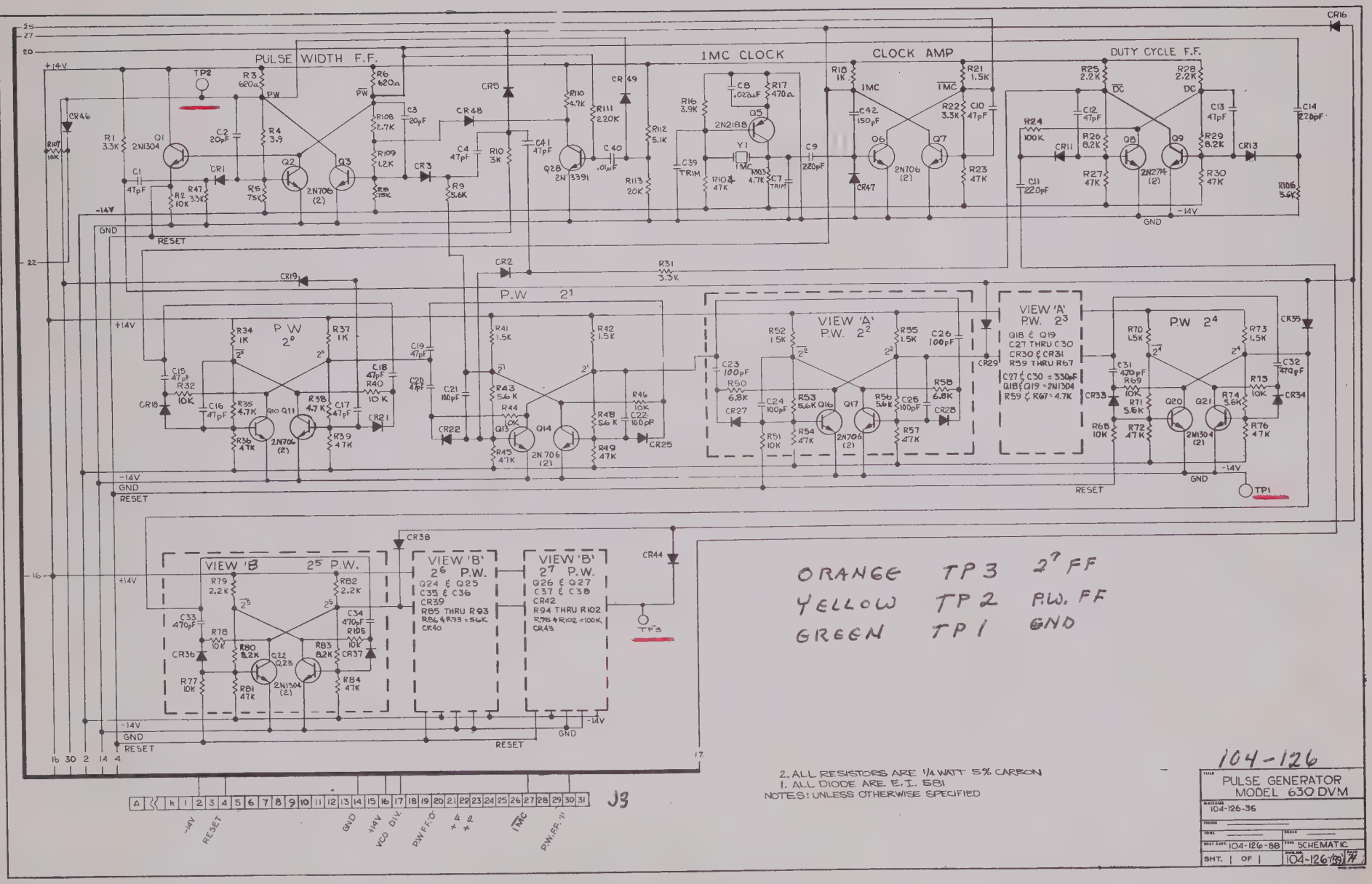
NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL TRANSISTORS ARE 2N1304
2. ALL DIODES ARE EI 581
3. ALL RESISTORS ARE ½ WATT 5% CARBON
4. R-15 & R-21 ARE MATCHED SET SPEC.# 015-143-17

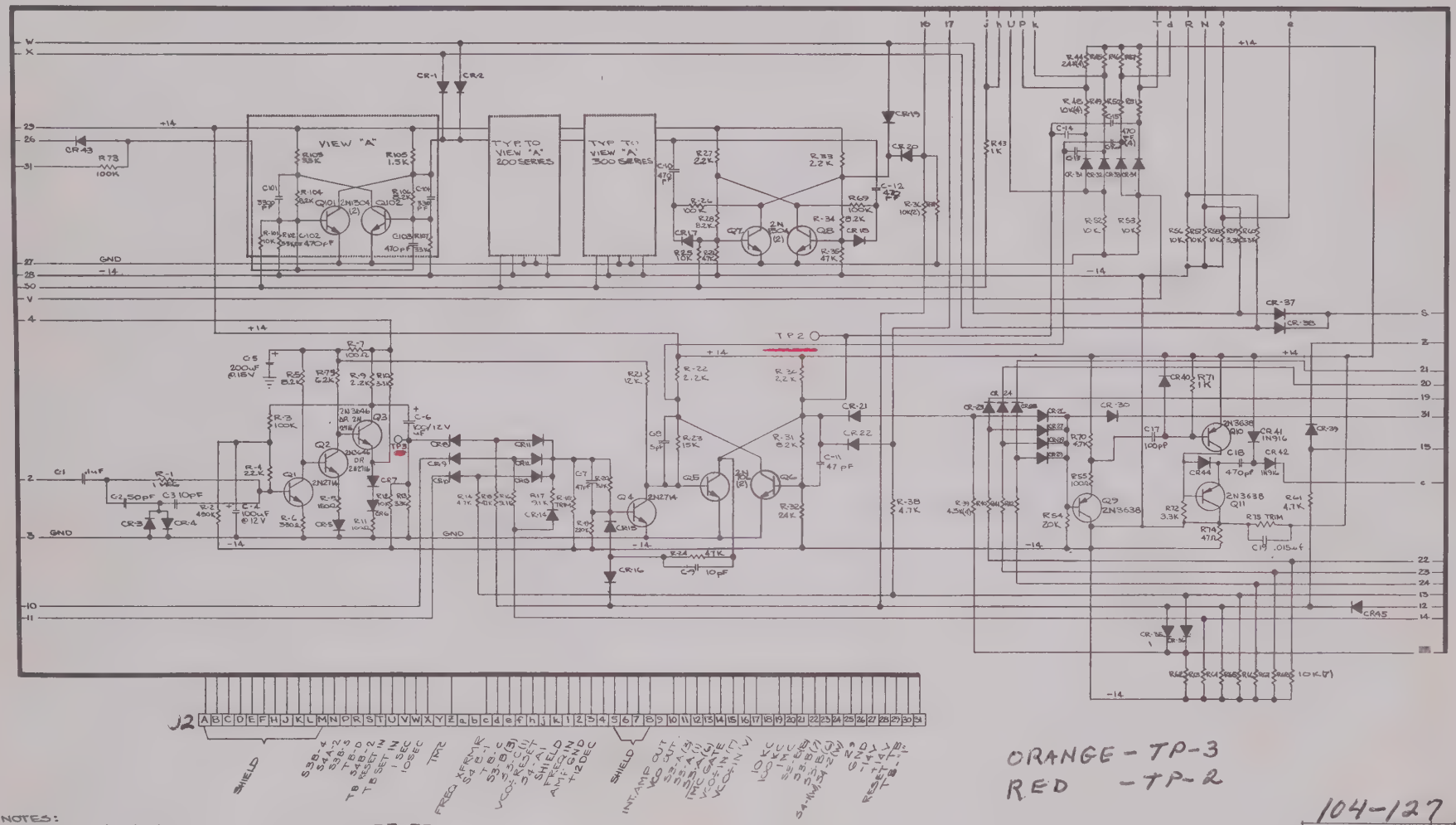
104-125

TITLE: INSIDE POWER SUPPLY 630 & 630S 104-125			
CODE IDENT NO. 00116	SIZE	DRAWING NO. 104-155-(80)	REV A
SCALE NONE	WEIGHT	SHEET 1 of 1	



TITLE: PRECISION REF SUPPLY RS-9			
CODE IDENT NO. 00116	SIZE C	DRAWING NO. 104-156-(80)	REV A
SCALE NONE	WEIGHT	SHEET 1 OF 1	

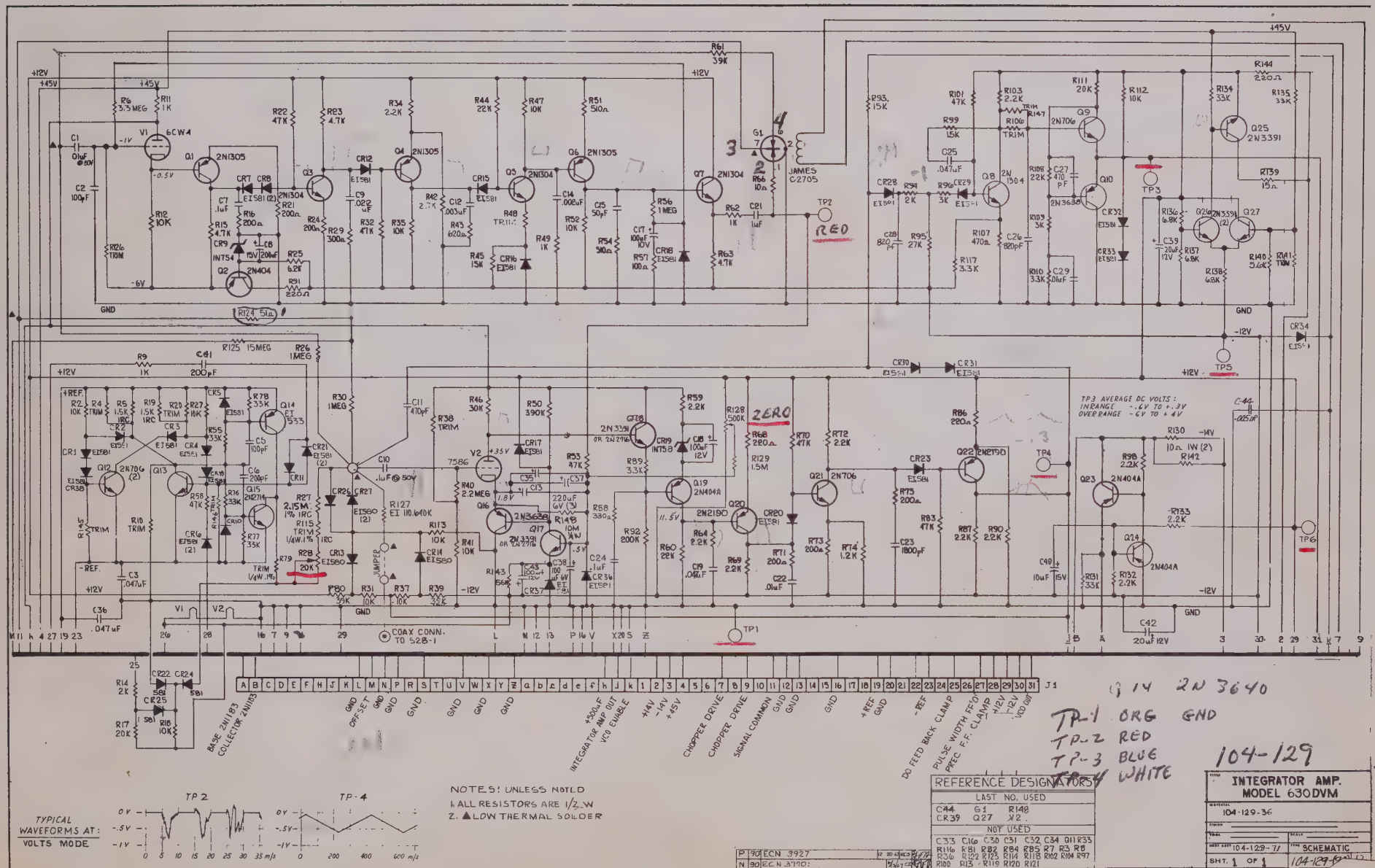

PULSE WIDTH F.F.
1MC CLOCK
CLOCK AMP
DUTY CYCLE F.F.
P.W 2°
P.W 2¹
VIEW 'A' P.W. 2²
VIEW 'A' P.W. 2³
P.W 2⁴
VIEW 'B' 2⁵ P.W.
VIEW 'B' 2⁶ P.W.
VIEW 'B' 2⁷ P.W.
Q18 & Q19
C27 THRU C30
CR30 & CR31
R59 THRU R67
C27 & C30 = 330pF
Q18 & Q19 = 2N1304
R59 & R67 = 4.7K
Q24 & Q25
C35 & C36
CR39
R85 THRU R93
R86 & R93 = 56K
CR40
Q26 & Q27
C37 & C38
CR42
R94 THRU R102
R95 & R102 = 100K
CR43
+14V
-14V
GND
RESET
TP1
TP2
TP3
J3
ORANGE TP3 2⁷ FF
YELLOW TP2 P.W. FF
GREEN TP1 GND
2. ALL RESISTORS ARE 1/4 WATT 5% CARBON
1. ALL DIODE ARE E.I. 581
NOTES: UNLESS OTHERWISE SPECIFIED
104-126
PULSE GENERATOR
MODEL 630 DVM
104-126-36
104-126-86
SCHEMATIC
104-126-(39)
SHT. 1 OF 1

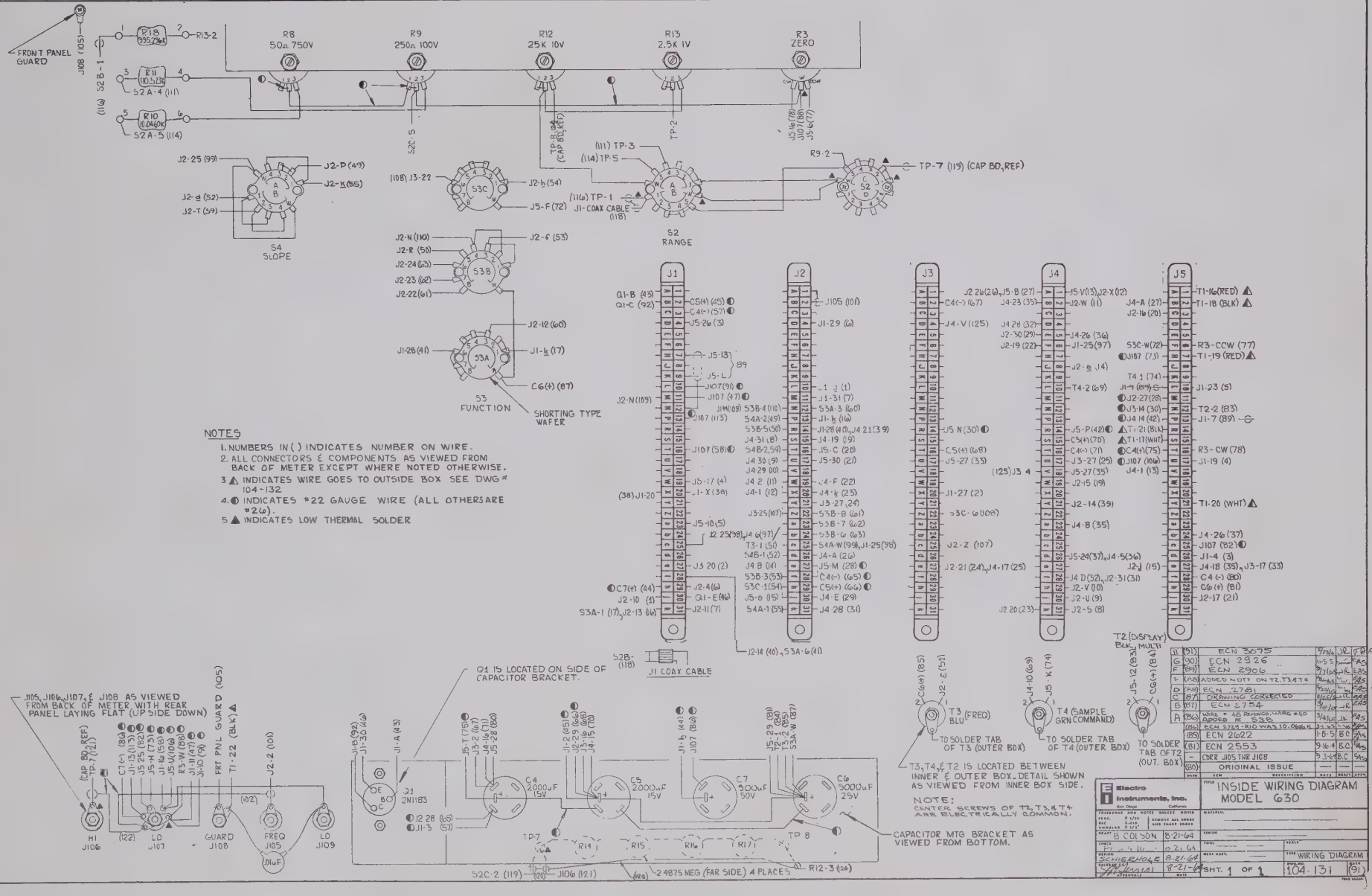


NOTES:
UNLESS OTHERWISE SPECIFIED ALL DIODES ARE E.I. 501
UNLESS OTHERWISE SPECIFIED ALL RESISTORS A 1/4 WATT, 5%

104-127

TITLE	FREQUENCY BD. MODEL 630 & 630S		
MATERIAL	104-127-39		
FINISH			
TOOL		SCALE	
NEXT ASY	104-127-89	TYPE	SCHEMATIC
SHT. 1 OF 1		DRAWING NO.	104-127


+12V
+45V
-6V
-12V
GND
-14V
V1 6CW4
V2 7586
Q1 2N1305
Q2 2N404
Q3 2N1304
Q4 2N1305
Q5 2N1304
Q6 2N1305
Q7 2N1304
G1 JAMES C-2705
Q8 2N1304
Q9 2N706
Q10 2N3638
Q25 2N3391
Q26 2N3391 (2)
Q27
Q12 2N706 (2)
Q13
Q14 EI 533
Q15 2N2714
Q16 2N3638
Q17 2N3391 OR 2N2714
Q18 2N3391 OR 2N2946
Q19 2N404A
Q20 2N2190
Q21 2N706
Q22 2N2190
Q23 2N404A
Q24 2N404A
TP1
TP2
TP3
TP4
TP5
TP6
RED
ZERO
TP3 AVERAGE DC VOLTS :
INRANGE -.6V TO +.3V
OVERRANGE -6V TO +4V
COAX CONN. TO 528-1
JUMPER
TRIM
TRIM 1/4W 1%
2.15M 1% 1RC
10M 1/4W
20K
J1
A B C D E F H J K L M N P R S T U V W X Y Z a b c d e f h J k 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
GND
OFF-SET
+500uF INTEGRATOR AMP OUT
VCO ENABLE
+14V
-14V
+45V
CHOPPER DRIVE
CHOPPER DRIVE
SIGNAL COMMON
+REF
-REF
DO FEED BACK CLAMP
PULSE WIDTH FF'S
PREC F.F. CLAMP
+12V
-12V
VCO OUT
BASE 2N1183
COLLECTOR 2N1183
TP 2
TP-4
0V
-.5V
-1V
0 5 10 15 20 25 30 35 m/s
0 200 400 600 m/s
TYPICAL WAVEFORMS AT: VOLTS MODE
NOTES: UNLESS NOTED
1. ALL RESISTORS ARE 1/2 W
2. ▲ LOW THERMAL SOLDER
REFERENCE DESIGNATORS
LAST NO. USED
C44 G1 R148
CR39 Q27 X2
NOT USED
C33 C116 C30 C31 C32 C34 Q11 R35
R116 R81 R82 R84 R85 R7 R3 R8
R36 R122 R123 R114 R113 R102 R104 R97
R100 R13 R119 R120 R121
P 90 ECN 3927
N 90 ECN 3770:
Q 14 2N 3640
TP-1 ORG GND
TP-2 RED
TP-3 BLUE
TP-4 WHITE
104-129
INTEGRATOR AMP. MODEL 630DVM
104-129-36
104-129-71
SCHEMATIC
SHT. 1 OF 1
104-129-Rev D



H	(91)	ECN 3075	9/7/66	JR	BC
G	(90)	ECN 2926	11-5-65	JR	EAS
F	(89)	ECN 2906	9/21/65	JR	EAS
E	(88)	ADDED NOTE ON T2, T3 & T4	8/26/65	JR	EAS
D	(86)	ECN 2781	8/2/65	JR	EAS
C	(85)	DRAWING CORRECTED	8/22/65	JR	EAS
B	(83)	ECN 2754	3/10/65	JR	EAS
A	(82)	WIRE * 48 CHANGED WIRE #110 ADDED TO #5336	3/4/65	JR	EAS
	(80)	ECN 3329 - R10 WAS 10.066K	3-1-65	JR	BC
	(85)	ECN 2622	1-15-65	BC	EAS
	(81)	ECN 2553	9-16-64	BC	EAS
	-	CHGE J105 THR J108	9-3-64	BC	EAS
	(80)	ORIGINAL ISSUE	---	---	---
	BASE	ECN	DESCRIPTION	DATE	DRAFT	APPV

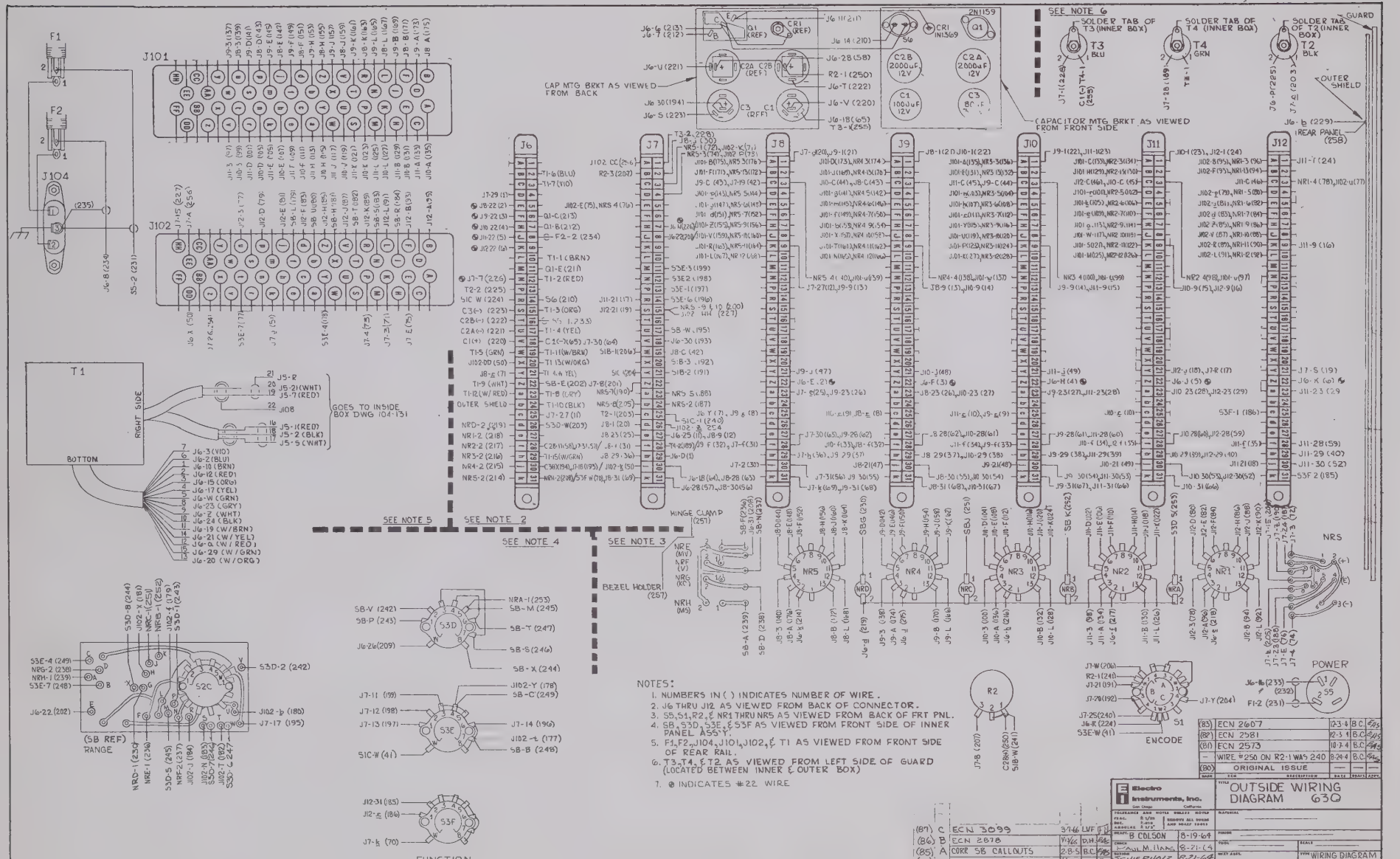
Electro Instruments, Inc. San Diego, California

TOLERANCE AND NOTES UNLESS NOTED: DEC. ± .X/30 BIC ± .XX/5 ANGULAR ± 1/2° — REMOVE ALL BURRS AND SHARP EDGES

DRAWN B COLSON 8-21-64
CHECK [illegible] 8-21-64
DESIGN SCHIERHOLZ 8-21-64
ENGINEER [illegible] 8-21-64
APPROVALS — DATE

MATERIAL —
FINISH —
TOOL —
MFGR ASSY. —
SCALE —
TYPE WIRING DIAGRAM
DWG. NO. 104-131
SHT. 1 OF 1
(91)

TITLE: INSIDE WIRING DIAGRAM MODEL G30



NOTES:

1. NUMBERS IN ( ) INDICATES NUMBER OF WIRE.
2. J6 THRU J12 AS VIEWED FROM BACK OF CONNECTOR.
3. S5, S1, R2, & NR1 THRU NR5 AS VIEWED FROM BACK OF FRT PNL.
4. SB, S3D, S3E, & S3F AS VIEWED FROM FRONT SIDE OF INNER PANEL ASS'Y.
5. F1, F2, J104, J101, J102, & T1 AS VIEWED FROM FRONT SIDE OF REAR RAIL.
6. T3, T4, & T2 AS VIEWED FROM LEFT SIDE OF GUARD (LOCATED BETWEEN INNER & OUTER BOX)
7. @ INDICATES #22 WIRE

(87)	C	ECN 3099	3/16	LVF
(86)	B	ECN 2878	1/16	D.H
(85)	A	CORE SB CALLOUTS	2-8-5	B.C
(85)		ECN 2602	1/64	
(84)		ECN 2620	N/A	

(83)	ECN 2607	12-3-64	B.C.
(82)	ECN 2581	12-3-64	B.C.
(81)	ECN 2573	10-7-64	B.C.
-	WIRE #250 ON R2-1 WAS 240	8-24-64	B.C.
(80)	ORIGINAL ISSUE		

Electro Instruments, Inc.	San Diego, California
DRAWN	B COLSON 8-19-64
CHKD	Paul M. Hans 8-21-64
ENGR	
APPROVED	
TOLERANCE AND NOTES UNLESS NOTED FRAC. ±1/64, DEC. ±.010, ANGULAR ±1/2°	
MATERIAL	
FINISH	
TOOL	
NEXT ASSY.	
SCALE	
TITLE	OUTSIDE WIRING DIAGRAM 630
TYPE	WIRING DIAGRAM
SHT. 1 OF 1	104-132-(87) C

HONEYWELL
INC.

WARRANTY

The Company warrants all equipment manufactured by it and bearing its name plate to be free from defects in workmanship and material, under normal use and service, as follows: (a) equipment not installed by the company which (i) is returned to the Company's originating factory within 12 months after date of shipment, and (ii) is found by the Company's inspection to be defective in workmanship or material, will be repaired or replaced free of charge and returned—shipped lowest-cost transportation prepaid; and (b) equipment installed by the Company which is within 12 months after date of installation by the Company found by the Company's inspection to be defective in workmanship or material, will be repaired or replaced free of charge. If inspection by the Company does not disclose any defect in workmanship or material, the Company's regular charges will apply. Items specifically excluded from the 12 month warranty and which will not be repaired or replaced free of charge include flash tubes, galvanometer lamps, indicating galvanometer suspensions, choppers, tubes, fuses, batteries and similar components subject to wear or burn-out through usage. Warranty on tape heads is limited to 90 days. All statutory and implied warranties, except of title, are negative and excluded. The foregoing provisions are in lieu of all other warranties, guarantees, obligations or liabilities on the part of the Company. The Company shall not be liable for and the purchaser assumes and will indemnify and save harmless the Company in respect to any loss or damage that may arise through the use by the purchaser or others of any of the equipment.

TEST INSTRUMENTS DIVISION SAN DIEGO OPERATION 8611 BALBOA AVENUE
SAN DIEGO, CALIFORNIA 92112 PHONE (714) 277-6590

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